Phison Electronics Corporation

PS3111-S11 Half Slim (Standard MO-297) TLC Specification

Version 1.3

Phison Electronics Corporation

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1.1	2016/06/15	Update performance and power consumption	Joe Leng
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1.3	2017/12/21	Update performance and power consumption	Wayne Chen

Product Overview

- **Capacity**
  - 30/32 GB up to 960/1024GB [Note2]
- **SATA Interface**
  - SATA Revision 3.2
  - SATA 1.5Gbps, 3Gbps, and 6Gbps interface
- **Flash Interface**
  - Flash type: TLC
  - 1pcs to 4pcs of TSOP flash
- **Performance**
  - Read: up to 550 MB/s
  - Write: up to 490 MB/s
- **Power Consumption** [Note1]
  - Active mode: < 1,945 mW
  - Idle mode: < 325 mW
  - DEVSLP mode: < 5 mW
- **MTBF**
  - More than 2,000,000 hours
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - TRIM
  - SMART
  - Over-Provision
  - Firmware Update
  - SmartZIP™
- **Low Power Management**
  - DEVSLP Mode (Optional)
  - DIPM/HIPM Mode
- **Temperature Range**
  - Operation: 0°C ~ 70°C
  - Storage: -40°C ~ 85°C
- **RoHS compliant**

Notes:

1. Please see “4.2 Power Consumption” for details.
2. Other capacities can be supported in the future.

Performance and Power Consumption

Capacity	Flash Structure	Performance				Power Consumption		
		CrystalDiskMark		ATTO		Read (mW)	Write (mW)	DEVSLP (mW)
		Read (MB/s)	Write (MB/s)	Read (MB/s)	Write (MB/s)			
120/128GB	64GBx2, TSOP, TSB Bics2	550	360	560	540	1,365	1,420	4.9
240/256GB	64GBx4, TSOP, TSB Bics2	550	490	560	540	1,430	1,720	4.9
120/128GB	32GBx4, TSOP, TSB 15nm	550	450	550	540	1,280	1,830	4.9
240/256GB	64GBx4, TSOP, TSB 15nm	550	450	550	540	1,525	1,945	4.9
30/32GB	32GBx1, TSOP, TSB Bics3	300	125	560	540	970	880	4.9
60/64GB	32GBx2, TSOP, TSB Bics3	550	255	560	540	1,230	1,000	4.9
120/128GB	64GBx2, TSOP, TSB Bics3	550	450	560	540	1,260	1,350	4.9
240/256GB	64GBx4, TSOP, TSB Bics3	550	490	560	540	1,330	1,450	4.9
240/256GB	128GBx2, TSOP, TSB Bics3	550	490	560	540	1,270	1,490	4.9

NOTE:

For more details on Power Consumption, please refer to Chapter 4.2.

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1. INTRODUCTION

1.1. General Description

Phison's PS3111 Half Slim delivers all the advantages of flash disk technology with Serial ATA I/II/III interface, including being fully compliant with standard 2.5-inch form factor, providing low power consumption compared to traditional hard drive and hot-swapping when removing/replacing/upgrading flash disks. The device is designed based on the standard 7-pin interface for data segment and 15-pin for power segment, as well as operating at a maximum operating frequency of 200MHz with 30MHz external crystal. Its capacity could provide a wide range up to 1024GB. Moreover, it can reach up to 550MB/s read as well as 500MB/s write high performance based on 16CE and Toggle 2.0 MLC flash (with 32MB SDR enabled and measured by CrystalDiskMark v5.0).

1.2. Controller Block Diagram

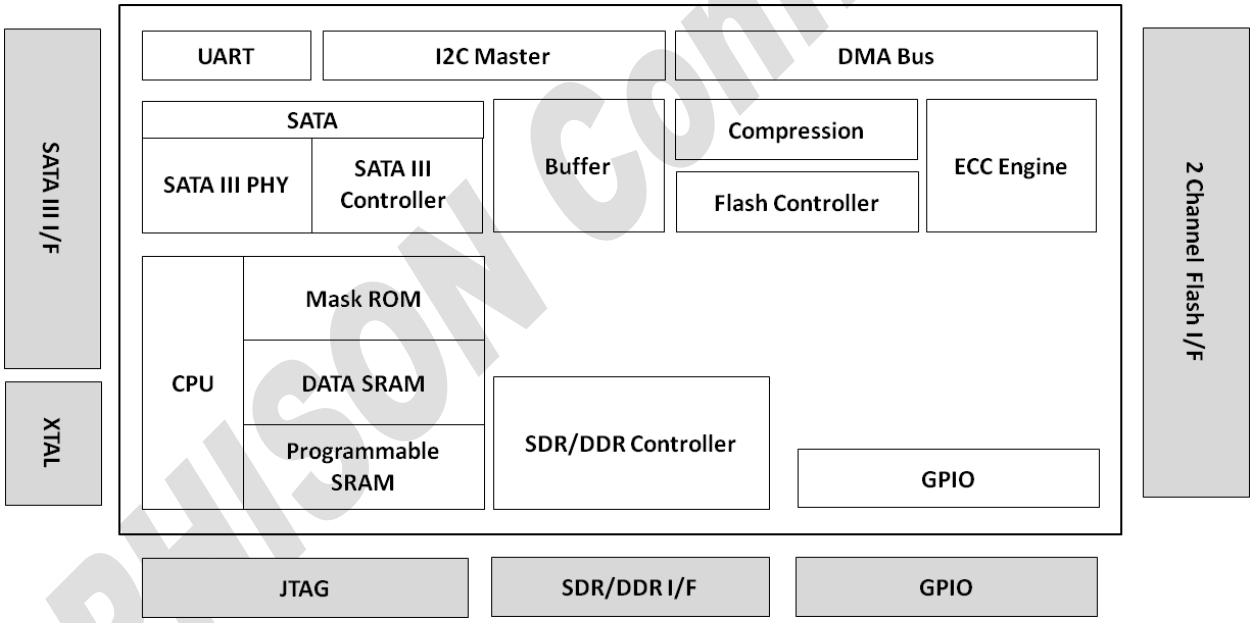


Figure 1-1 PS3111 Half Slim Controller Block Diagram

1.3. Product Block Diagram

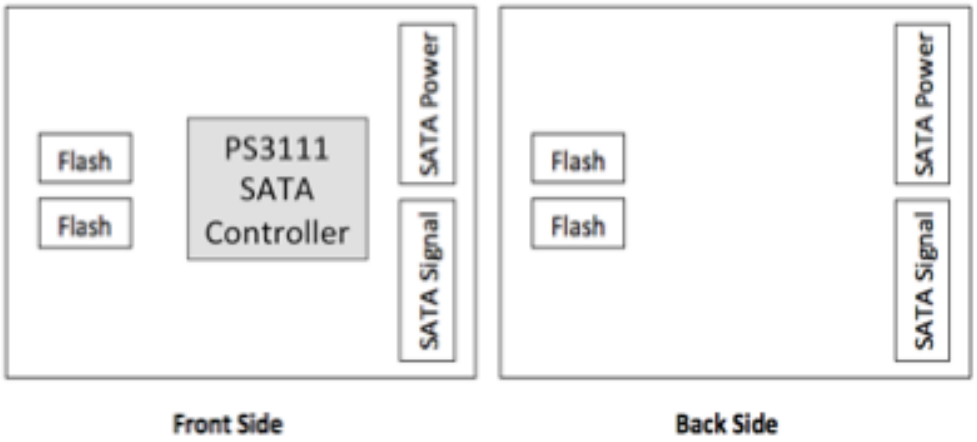


Figure 1-2 PS3111 Half Slim Product Block Diagram

1.4. Flash Management

1.4.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, PS3111 Half Slim applies the LDPC (Low Density Parity Check) of ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

1.4.2. Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND flash by evenly distributing write and erase cycles across the media.

Phison provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.4.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Phison implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.4.4. TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

1.4.5. SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

1.4.6. Over-Provision

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

1.4.7. Firmware Upgrade

Firmware can be considered as a set of instructions on how the device communicates with the host.

Firmware will be upgraded when new features are added, compatibility issues are fixed, or read/write performance gets improved.

1.5. Low Power Management

1.5.1. DEVSLP Mode (Optional)

With the increasing need of aggressive power/battery life, SATA interfaces include a new feature, Device Sleep (DEVSLP) mode, which helps further reduce the power consumption of the device. DEVSLP enables the device to completely power down the device PHY and other sub-systems, making the device reach a new level of lower power operation. The DEVSLP does not specify the exact power level a device can achieve in the DEVSLP mode, but the power usage can be dropped down to 5mW or less.

1.5.2. DIPM/HIPM Mode

SATA interfaces contain two low power management states for power saving: Partial and Slumber modes. For Partial mode, the device has to resume to full operation within 10 microseconds, whereas the device will spend 10 milliseconds to become fully operational in the Slumber mode. SATA interfaces allow low power modes to be initiated by Host (HIPM, Host Initiated Power Management) or Device (DIPM, Device Initiated Power Management). As for HIPM, Partial or Slumber mode can be invoked directly by the software. For DIPM, the device will send requests to enter Partial or Slumber mode.

1.6. Power Loss Protection: Flushing Mechanism (Optional)

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, the PS3111 applies the ***GuaranteedFlush*** technology, which requests the controller to transfer data to the cache. For PS3111, SDR performs as a cache, and its size is 32MB. Only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

Additionally, it is critical for a controller to shorten the time the in-flight data stays in the cache. Thus, Phison's PS3111 applies an algorithm to reduce the amount of data resides in the cache to provide a better

performance. This ***SmartCacheFlush*** technology allows incoming data to only have a “pit stop” in the cache and then move to the NAND flash at once. If the flash is jammed due to particular file sizes (such as random 4KB data), the cache will be treated as an “organizer”, consolidating incoming data into groups before written into the flash to improve write amplification.

In sum, with Flush Mechanism, PS3111 proves to provide the reliability required by consumer, industrial, and enterprise-level applications.

1.7. Advanced Device Security Features

1.7.1. Secure Erase

Secure Erase is a standard ATA command and will write all “0xFF” to fully wipe all the data on hard drives and SSDs. When this command is issued, the SSD controller will erase its storage blocks and return to its factory default settings.

1.7.2. Write Protect

When a SSD contains too many bad blocks and data are continuously written in, then the SSD might not be usable anymore. Thus, Write Protect is a mechanism to prevent data from being written in and protect the accuracy of data that are already stored in the SSD.

1.8. SSD Lifetime Management

1.8.1. Thermal Monitor (Optional)

Thermal monitors are devices for measuring temperature, and can be found in SSDs in order to issue warnings when SSDs go beyond a certain temperature. The higher temperature the thermal monitor detects, the more power the SSD consumes, causing the SSD to get aging quickly. Hence, the processing speed of a SSD should be under control to prevent temperature from exceeding a certain range. Meanwhile, the SSD can achieve power savings.

1.9. An Adaptive Approach to Performance Tuning

1.9.1. Throughput

Based on the available space of the disk, PS3111 will regulate the read/write speed and manage the

performance of throughput. When there still remains a lot of space, the firmware will continuously perform read/write action. There is still no need to implement garbage collection to allocate and release memory, which will accelerate the read/write processing to improve the performance. Contrarily, when the space is going to be used up, PS3111 will slow down the read/write processing, and implement garbage collection to release memory. Hence, read/write performance will become slower.

1.9.2. Predict & Fetch

Normally, when the host tries to read data from the SSD, the SSD will only perform one read action after receiving one command. However, PS3111 applies ***Predict & Fetch*** to improve the read speed. When the host issues sequential read commands to the SSD, the SSD will automatically expect that the following will also be read commands. Thus, before receiving the next command, flash has already prepared the data. Accordingly, this accelerates the data processing time, and the host does not need to wait so long to receive data.

1.9.3. SmartZIP™

Write data to the NAND Flash costs time. To improve the write speed performance, PS3111 launches with compression technique—SmartZIP™

Whether a file could be compressed or not depending on the file type, for file types have redundancy data pattern, through our embedded encode engine, we could reduce the amount of data that is actually written to the Flash. Comparing to the SSD without the compression, write efficiency is raised and the SSD endurance is also improved since Flash could be benefit from less data written for a longer SSD lifetime.

2. PRODUCT SPECIFICATIONS

- **Capacity**
  - From 30/32GB up to 960/1024GB (support 48-bit addressing mode)
- **Electrical/Physical Interface**
  - SATA Interface
    - Compliant with SATA Revision 3.2
    - Compatible with SATA 1.5Gbps, 3Gbps and 6Gbps interface
    - Support power management
    - Support expanded register for SATA protocol 48 bits addressing mode
    - Embedded BIST function for SATA PHY for low cost mass production
- **Built-in 2-channel NAND flash interface controller**
  - Compliant with Toggle 1.0 and Toggle 2.0 NAND Flash interface
  - Compliant with ONFI 4.0 interface:
    - SDR up to mode 5
    - NV-DDR up to mode 5
    - NV-DDR2 up to mode 7
    - NV-DDR3 up to mode 8
- **Supported NAND Flash**
  - Support up to 16 Flash Chip Enables (CE) within single design
  - Toshiba 24nm SLC; 15nm/3D-NAND MLC; 15nm/3D-NAND TLC
  - Intel/Micron/Spectek 16nm/3D-NAND MLC and TLC
  - Hynix 16nm/3D-NAND
  - Support all types of SLC/MLC/TLC/3D-NAND, 8KB/page and 16K/page NAND flash
  - Support ONFI 2.3, ONFI 3.0, ONFI 3.2 and ONFI 4.0 interface: 2 channels at maximum
  - Support 8-bit I/O NAND Flash
  - Contain 1pcs to 4pcs of TSOP flash
- **ECC Scheme**
  - PS3111 Half Slim applies the LDPC (Low Density Parity Check) of ECC algorithm.
- **UART function**
- **GPIO**
- **Support SMART and TRIM commands**

- **Performance**

Capacity	Flash Structure	Flash Type	Sequential	
			Read (MB/s)	Write (MB/s)
120/128GB	64GB x 2	TSOP, TSB Bics2	550	360
240/256GB	64GB x 4	TSOP, TSB Bics2	550	490
120/128GB	32GB x 4	TSOP, TSB 15nm	550	450
240/256GB	64GB x 4	TSOP, TSB 15nm	550	450
30/32GB	32GBx1	TSOP, TSB Bics3	300	125
60/64GB	32GBx2	TSOP, TSB Bics3	550	255
120/128GB	64GBx2	TSOP, TSB Bics3	550	450
240/256GB	64GBx4, 128GBx2	TSOP, TSB Bics3	550	490

NOTES:

1. The performance was measured using CrystalDiskMarkv5.0x64 with SATA 6Gbps host.
2. Samples were built using Toshiba 15nm and Bics2/Bics3 TLC NAND.
3. Performance may differ according to flash configuration and platform.
4. The table above is for reference only. The criteria for MP (mass production) and for accepting goods shall be discussed based on different flash configuration.

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

- Temperature:
  - Storage: -40°C to 85°C
  - Operational: 0°C to 70°C
- Humidity: RH 90% under 40°C (operational)

Table 3-1 High Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	70°C	0% RH	72 hours
Storage	85°C	0% RH	72 hours

Result: No any abnormality is detected.

Table 3-2 Low Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	0°C	0% RH	72 hours
Storage	-40°C	0% RH	72 hours

Result: No any abnormality is detected.

Table 3-3 High Humidity Test Condition

	Temperature	Humidity	Test Time
Operation	40°C	90% RH	4 hours
Storage	40°C	93% RH	72 hours

Result: No any abnormality is detected.

Table 3-4 Temperature Cycle Test

	Temperature	Test Time	Cycle
Operation	0°C	30 min	10 Cycles
	70°C	30 min	
Storage	-40°C	30 min	10 Cycles
	85°C	30 min	

Result: No any abnormality is detected.

3.1.2. Shock

Table 3-5 PS3111 Half Slim Shock Specification

	Acceleration Force	Half Sin Pulse Duration
Non-operational	1500G	0.5ms

Result: No any abnormality is detected when power on.

3.1.3. Vibration

Table 3-6 PS3111 Half Slim Vibration Specification

	Condition		Vibration Orientation
	Frequency/Displacement	Frequency/Acceleration	
Non-operational	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G	X, Y, Z axis/60 min for each

Result: No any abnormality is detected when power on.

3.1.4. Drop

Table 3-7 PS3111 Half Slim Drop Specification

	Height of Drop	Number of Drop
Non-operational	80cm free fall	6 face of each unit

Result: No any abnormality is detected when power on.

3.1.5. Bending

Table 3-8 PS3111 Half Slim Bending Specification

	Force	Action
Non-operational	≥ 50N	Hold 1min/5times

Result: No any abnormality is detected when power on.

3.1.6. Torque

Table 3-9 PS3111 Half Slim Torque Specification

	Force	Action
Non-operational	1.263N-m or ±10 deg	Hold 1min/5times

Result: No any abnormality is detected when power on.

3.1.7. Electrostatic Discharge (ESD)

Table 3-10 PS3111 Half Slim Contact ESD Specification

Device	Capacity	Temperature	Relative Humidity	+/- 4KV	Result
Half Slim	256GB	24.0°C	49% (RH)	Device functions are affected, but EUT will be back to its normal or operational state automatically.	PASS
	512GB				

3.1.8. EMI Compliance

- FCC: CISPR22
- CE: EN55022
- BSMI 13438

3.2. MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of Phison's PS3111 Half Slim is more than 2,000,000 hours.

3.3. Certification & Compliance

- RoHS
- SATA III (SATA Rev. 3.2)
- Up to ATA/ATAPI-8 (Including S.M.A.R.T)

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage

Table 4-1 Supply Voltage of PS3111 Half Slim

Parameter	Rating
Operating Voltage	5V

4.2. Power Consumption

Table 4-2 Power Consumption of PS3111 Half Slim

Capacity	Flash Structure	Flash Type	Read (mW)	Write (mW)	Partial (mW)	Slumber (mW)	Idle (mW)	DEVSLP (mW)
120/128GB	64GB x 2	TSOP, TSB Bics2	1,365	1,420	19	15	315	4.9
240/256GB	64GB x 4	TSOP, TSB Bics2	1,430	1,720	19	15	315	4.9
120/128GB	32GB x 4	TSOP, TSB 15nm	1,280	1,830	12	7	285	4.9
240/256GB	64GB x 4	TSOP, TSB 15nm	1,525	1,945	13.5	8	315	4.9
30/32GB	32GB x 1	TSOP, TSB Bics3	970	880	22.5	15.5	325	4.9
60/64GB	32GB x 2	TSOP, TSB Bics3	1,230	1,000	20	14	320	4.9
120/128GB	64GB x 2	TSOP, TSB Bics3	1,260	1,350	20	14	320	4.9
240/256GB	64GB x 4	TSOP, TSB Bics3	1,330	1,450	20	14	325	4.9
240/256GB	128GB x 2	TSOP, TSB Bics3	1,270	1,490	20.5	15	320	4.9

NOTES:

1. The average value of power consumption is achieved based on 100% conversion efficiency.
2. The measured power voltage is 5V.
3. Samples were built using Toshiba 15nm and Bics2/Bics3 TLC NAND.
   It's measured under ambient temperature.
4. Sequential R/W is measured while testing 4000MB sequential R/W 5 times by CyrstalDiskMark. DEVSLP is measured while entering device sleep mode for 5 minutes.
5. Power Consumption may differ according to flash configuration and platform.

5. INTERFACE

5.1. Pin Assignment and Descriptions

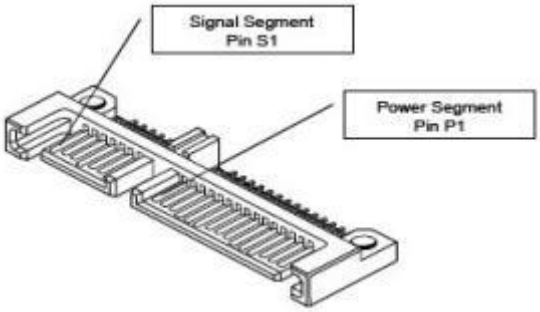


Figure 5-1 PS3111 Half Slim Pin Assignment

Table 5-1 Signal Segment Pin Assignment and Descriptions

Pin Number	Function
S1	GND
S2	A+ (Differential Signal Pair A)
S3	A – (Differential Signal Pair A)
S4	GND
S5	B – (Differential Signal Pair B)
S6	B+ (Differential Signal Pair B)
S7	GND

Table 5-2 Power Segment Pin Assignment and Descriptions

Pin Number	Function
P1	Not Used (3.3V)
P2	Not Used (3.3V)
P3	DEVSLP
P4	GND
P5	GND
P6	GND
P7	5V pre-charge
P8	5V
P9	5V
P10	GND
P11	Reserved
P12	GND
P13	Not Used (12V pre-charge)
P14	Not Used (12V)
P15	Not Used (12V)

6. SUPPORTED COMMANDS

6.1. ATA Command List

The following ATA command list table is followed by ATA8-ACS4 SPEC.

Table 6-1 ATA Command List

Op Code	Description	Op Code			Description
00h	NOP	C9h			Read DMA without Retry
06h	Data Set Management	CAh			Write DMA
10h-1Fh	Recalibrate	CBh			Write DMA without Retry
20h	Read Sectors	CEh			Write Multiple FUA EXT
21h	Read Sectors without Retry	E0h			Standby Immediate
24h	Read Sectors EXT	E1h			Idle Immediate
25h	Read DMA EXT	E2h			Standby
27h	Read Native Max Address EXT	E3h			Idle
29h	Read Multiple EXT	E4h			Read Buffer
2Fh	Read Log EXT	E5h			Check Power Mode
30h	Write Sectors	E6h			Sleep
31h	Write Sectors without Retry	E7h			Flush Cache
34h	Write Sectors EXT	E8h			Write Buffer
35h	Write DMA EXT	E9h			READ BUFFER DMA
37h	Set Native Max Address EXT	EAh			Flush Cache EXT
38h	CFA Write Sectors Without Erase	EBh			Write Buffer DMA
39h	Write Multiple EXT	ECh			Identify Device
3Dh	Write DMA FUA EXT	EFh			Set Features
3Fh	Write Long EXT	EFh	02h		Enable volatile write cache
40h	Read Verify Sectors	EFh	03h		Set transfer mode
41h	Read Verify Sectors without Retry	EFh	05h		Enable the APM feature set
42h	Read Verify Sectors EXT	EFh	10h		Enable use of SATA features et
44h	Zero EXT	EFh	10h	02h	Enable DMA Setup FIS Auto-Activate optimization
45h	Write Uncorrectable EXT	EFh	10h	03h	Enable Device-initiated interface power state (DIPM) transitions
47h	Read Log DMA EXT	EFh	10h	06h	Enable Software Settings Preservation (SSP)
57h	Write Log DMA EXT	EFh	10h	07h	Enable Device Automatic Partial to Slumber transitions
60h	Read FPDMA Queued	EFh	10h	09h	Enable Device Sleep
61h	Write FPDMA Queued	EFh	55h		Disable read look-ahead
70h-7Fh	Seek	EFh	66h		Disable reverting to power-on defaults

Op Code		Description	Op Code			Description
90h		Execute Device Diagnostic	EFh	82h		Disable volatile write cache
91h		Initialize Device Parameters	EFh	85h		Disable the APM feature set
92h		Download Microcode	EFh	90h		Disable use of SATA feature set
93h		Download Microcode DMA	EFh	90h	02h	Disable DMA Setup FIS Auto-Activate optimization
B0h		SMART	EFh	90h	03h	Disable Device-initiated interface power state (DIPM) transitions
B0h	D0h	SMART READ DATA	EFh	90h	06h	Disable Software Settings Preservation (SSP)
B0h	D1h	SMART READ ATTRIBUTE THRESHOLDS	EFh	90h	07h	Disable Device Automatic Partial to Slumber transitions
B0h	D2h	SMART ENABLE/DISABILE ATTRIBUTE AUTOSAVE	EFh	90h	09h	Disable Device Sleep
B0h	D3h	SMART SAVE ATTRIBUTE VALUES	EFh	AAh		Enable read look-ahead
B0h	D4h	SMART EXECUTE OFF-LINE IMMEDIATE	EFh	CCh		Enable reverting to power-on defaults
B0h	D5h	SMART READ LOG	F1h			Security Set Password
B0h	D6h	SMART WRITE LOG	F2h			Security Unlock
B0h	D8h	SMART ENABLE OPERATIONS	F3h			Security Erase Prepare
B0h	D9h	SMART DISABLE OPERATIONS	F4h			Security Erase Unit
B0h	DAh	SMART RETURN STATUS	F5h			Security Freeze Lock
B0h	DBh	SMART ENABLE/DISABILE AUTOMATIC OFF-LINE	F6h			Security Disable Password
B1h		Device Configuration	F8h			Read Native Max Address
B4h		Sanitize	F9h			Set Max Address
C4h		Read Multiple	F9h	01h		SET MAX SET PASSWORD
C5h		Write Multiple	F9h	02h		SET MAXLOCK
C6h		Set Multiple Mode	F9h	03h		SET MAX UNLOCK
C8h		Read DMA	F9h	04h		SET MAX FREEZE LOCIK

6.2. Identify Device Data

The following table details the sector data returned by the IDENTIFY DEVICE command of ATA8-ACS4 SPEC.

Table 6-2 List of Device Identification

Word	F: Fixed V: Variable X: retired/obsolete /reserved	Default Value	Description
0	F	0040h	General configuration bit-significant information
1	X	***1**	Obsolete
2	F	C837h	Specific configuration
3	X	0010h	Obsolete
4-5	X	00000000h	Retired
6	X	003Fh	Obsolete
7-8	X	00000000h	Reserved for assignment by the Compact Flash Association
9	X	0000h	Retired
10-19	V	Varies	Serial number (20 ASCII characters)
20-21	X	00000000h	Retired
22	X	0000h	Obsolete
23-26	V	Varies	Firmware revision (8 ASCII characters)
27-46	V	Varies	Model number (xxxxxxxx)
47	F	8010h	7:0- Maximum number of sectors transferred per interrupt on MULTIPLE commands
48	F	4000h	Trusted Computing feature set options(not support)
49	F	2F00h	Capabilities
50	F	4000h	Capabilities
51-52	X	000000000h	Obsolete
53	F	0007h	Words 88 and 70:64 valid
54	X	***1**	Obsolete
55	X	0010h	Obsolete
56	X	003Fh	Obsolete
57-58	X	***2**	Obsolete
59	F	5D10h	Sanitize and Number of sectors transferred per interrupt on MULTIPLE commands
60-61	V	***3**	Maximum number of sector (28bit LBA mode)
62	X	0000h	Obsolete

Word	F: Fixed V: Variable X: retired/obsolete /reserved	Default Value	Description
63	F	0407h	Multi-word DMA modes supported/selected
64	F	0003h	PIO modes supported
65	F	0078h	Minimum Multiword DMA transfer cycle time per word
66	F	0078h	Manufacturer's recommended Multiword DMA transfer cycle time
67	F	0078h	Minimum PIO transfer cycle time without flow control
68	F	0078h	Minimum PIO transfer cycle time with IORDY flow control
69	F	1F00h	Additional Supported (support download microcode DMA)
70	X	0000h	Reserved
71-74	X	0000000000000000h	Reserved for the IDENTIFY PACKET DEVICE command
75	F	001Fh	Queue depth
76	F	850Eh	Serial SATA capabilities
77	F	0006h	Serial ATA Additional Capabilities
78	F	004Ch	Serial ATA features supported
79	F	0040h	Serial ATA features enabled
80	F	0FF8h	Major Version Number
81	F	0000h	Minor Version Number
82	F	746Bh	Command set supported
83	F	7D01h	Command set supported
84	F	4163h	Command set/feature supported extension
85	F	7469h	Command set/feature enabled
86	F	BC01h	Command set/feature enabled
87	F	4163h	Command set/feature default
88	F	007Fh	Ultra DMA Modes
89	F	0003h	Time required for security erase unit completion
90	F	001Eh	Time required for Enhanced security erase completion
91	F	0000h	Current advanced power management value
92	F	FFFEh	Master Password Revision Code
93	F	0000h	Hardware reset result. For SATA devices, word 93 shall be set to the value 0000h.

Word	F: Fixed V: Variable X: retired/obsolete /reserved	Default Value	Description
94	X	0000h	Obsolete
95	F	0000h	Stream Minimum Request Size
96	F	0000h	Streaming Transfer Time – DMA
97	F	0000h	Streaming Access Latency – DMA and PIO
98-99	F	00000000h	Streaming Performance Granularity
100-103	V	***4**	Maximum user LBA for 48 bit Address feature set
104	F	0000h	Streaming Transfer Time – PIO
105	F	0008h	Maximum number of 512-byte blocks per DATA SET MANAGEMENT command
106	F	4000h	Physical sector size/Logical sector size
107	F	0000h	Inter-seek delay for ISO-7779 acoustic testing in microseconds
108-111	V	Varies	World Wide Name
112-115	X	0000000000000000h	Reserved
116	X	0000h	Reserved
117-118	F	00000000h	Words per logical Sector
119	F	401Ch	Supported settings
120	F	401Ch	Command set/Feature Enabled/Supported
121-126	X	0h	Reserved
127	X	0000h	Obsolete
128	F	0021h	Security status
129-140	V	Varies	Vendor specific
141	V	Varies	Vendor specific
142-159	V	Varies	Vendor specific
160	X	0000h	Reserved for CFA
161-167	X	0h	Reserved for CFA
168	V	Varies	Device Nominal Form Factor
169	F	0001h	DATA SET MANAGEMENT command is supported
170-173	F	0000000000000000h	Additional Product Identifier
174-175	X	00000000h	Reserved
176-205	F	0h	Current media serial number

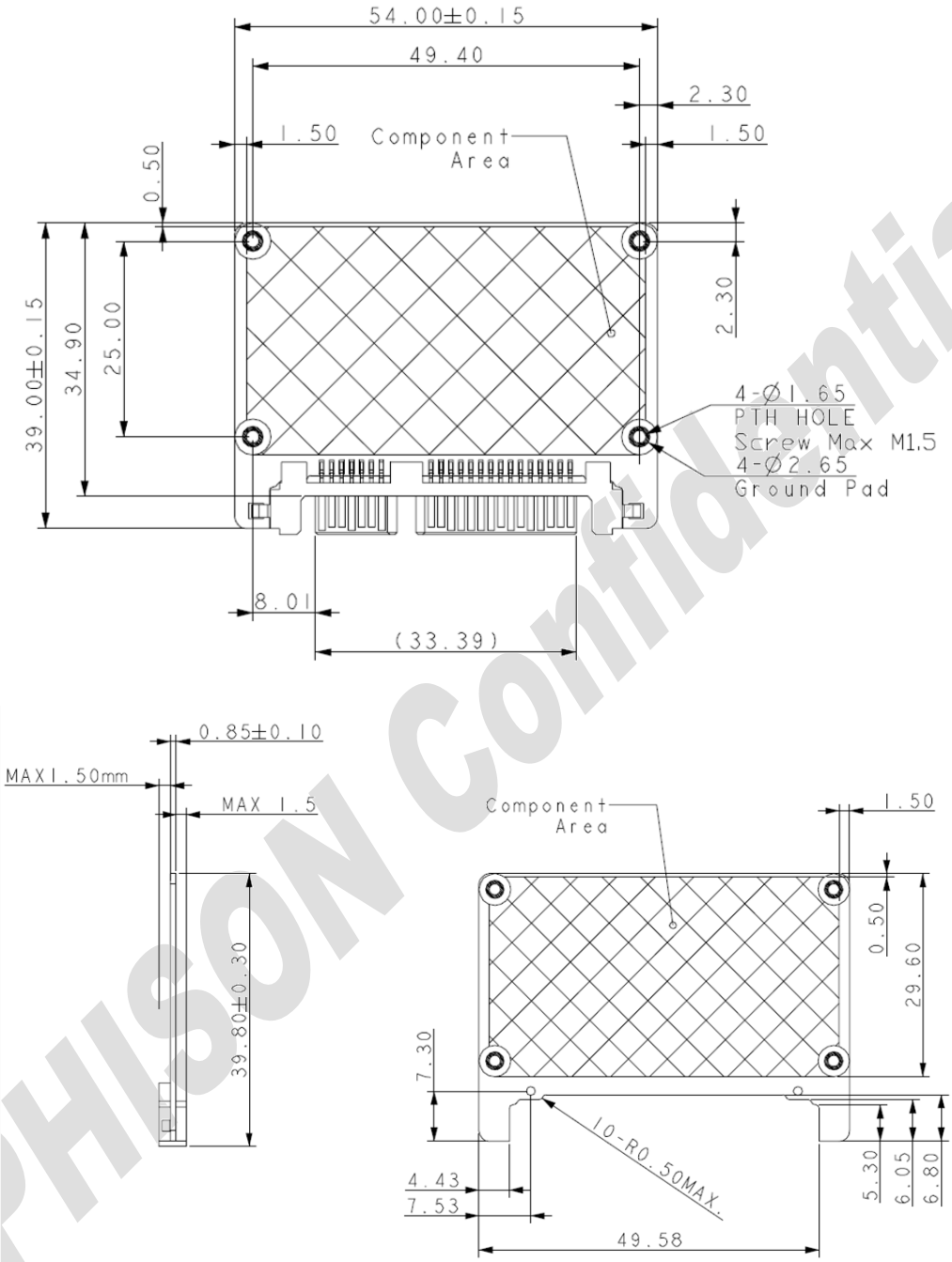
Word	F: Fixed V: Variable X: retired/obsolete /reserved	Default Value	Description
206	F	0000h	SCT Command Transport
207-208	X	00000000h	Reserved
209	F	4000h	Alignment of logical blocks within a physical block
210-211	F	00000000h	Write-Read-Verify Sector Count Mode 3 (not support)
212-213	F	00000000h	Write-Read-Verify Sector Count Mode 2 (not support)
214-216	X	0h	Obsolete
217	F	0001h	Non-rotating media device
218	X	0000h	Reserved
219	X	0000h	NV Cache relate (not support)
220	V	0000h	Write read verify feature set current mode
221	X	0000h	Reserved
222	F	10FFh	Transport major version number
223	F	0000h	Transport minor version number
224-229	X	0h	Reserved
230-233	F	000000000000 0000h	Extend number of user addressable sectors
234	F	0001h	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
235	F	FFFEh	Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
236-254	X	0h	Reserved
255	F	XXA5h XX is variable	Integrity word (Checksum and Signature)

Table 6-3 List of Device Identification for Each Capacity

Capacity (GB)	*1 (Word 1/Word 54)	*2 (Word 57 – 58)	*3 (Word 60 – 61)	*4 (Word 100 – 103)
120	3FFFh	FBFC10h	DF94BB0h	DF94BB0h
128	3FFFh	FBFC10h	EE7C2B0h	EE7C2B0h
240	3FFFh	FBFC10h	FFFFFFFh	1BF244B0h
256	3FFFh	FBFC10h	FFFFFFFh	1DCF32B0h

7. PHYSICAL DIMENSION

Dimension: 54mm (L) x 39mm (W) x 4.00mm (H)



Notes :
1. ▨ = Max Component Height
2. ▨ = No Component
3. ▨ = No Component/Signal Vias/Signal Copper/Printing
4. General Tolerance ± 0.1mm
5. Check Point:
6. Allowed burr (允許毛邊) Max.0.1mm.
7. Screw Max Size, M1.5

8. PRODUCT WARRANTY POLICY

In the event the Product does not conform to the specification within Phison agreed warranty period and such inconformity is solely attributable to Phison's cause, Phison agrees at its discretion replace or repair the nonconforming Product. Notwithstanding the foregoing, the aforementioned warranty shall exclude the inconformity arising from, in relation to or associated with:

(1) alternation, modification, improper use, misuse or excessive use of the Product;

(2) failure to comply with Phison's instructions;

(3) Phison's compliance with customer (including customer's suppliers, subcontractors or downstream customers) indicated instructions, technologies, designs, specifications, materials, components, parts;

(4) combination of the Product with other materials, components, parts, goods, hardware, firmware or software not developed by Phison; or

(5) other error or failure not solely attributable to Phison's cause (including without limitation, normal wear or tear, manufacturing or assembly wastage, improper operation, virus, unauthorized maintenance or repair).

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9. REFERENCE

The following table is to list out the standards that have been adopted for designing the product.

Table 9-1 List of References

Title	Acronym/Source
RoHS	Restriction of Hazardous Substances Directive; for further information, please contact us at sales@phison.com or support@phison.com.
Serial ATA Revision 3.2	http://www.sata-io.org
ATA-8 spec	http://www.t13.org
FCC: CISPR22	Federal Communications Commission; for further information, please contact us at sales@phison.com or support@phison.com.
CE: EN55022	Consumer electronics certification; for further information, please contact us at sales@phison.com or support@phison.com.
BSMI: 13438	The Bureau of Standards, Metrology and Inspection; for further information, please contact us at sales@phison.com or support@phison.com.

10. TERMINOLOGY

The following table is to list out the acronyms that have been applied throughout the document.

Table 10-1 List of Terminology

Term	Definitions
ATTO	Commercial performance benchmark application
DEVSLP	Device sleep mode
DIPM	Device initiated power management
HIPM	Host initiated power management
LBA	Logical block addressing
MB	Mega-byte
MTBF	Mean time between failures
NCQ	Native command queue
SATA	Serial advanced technology attachment
SDR	Synchronous dynamic access memory
S.M.A.R.T.	Self-monitoring, analysis and reporting technology
SSD	Solid state disk