Phison Electronics Corporation

PS3016-P9 CompactFlash Card Specification

Version 1.4

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Revision History

Revision	Release Date	History	Author
1.0	2014/01/9	First release	Rick Chen
1.1	2014/02/18	Adjust Performance/TBW/Power Consumption data	Rick Chen
1.2	2014/08/27	Update Performance/TBC/Power Consumption for TSB A19nm NAND Flash	Stevens Lin
1.3	2014/9/26	Update Pin Assignment and Descriptions	Stevens Lin
1.4	2015/9/30	Update 15nm NAND Flash solution of performance	Stevens Lin

Product Overview

- **Capacity**
  - 512MB up to 128GB
- **Host Interface**
  - PCMCIA/IDE interface
  - CompactFlash Specification Ver 3.x, 4.x, 5.x and 6.x
  - PC Card Standard Release 8.0
- **Flash Interface**
  - Flash Type: SLC, MLC, Pseudo SLC
  - 4KB/8KB/16KB per page NAND flash
- **Performance** [Note1]
  - Read: up to 105MB/s
  - Write: up to 80 MB/s
- **Power Consumption** [Note2]
  - Active mode: < 945mW
  - Idle mode: < 5mW
- **TBW (Terabytes Written)** [Note3]
  - 69 TBW for 128GB
- **MTBF**
  - More than 1,000,000 hours
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - Firmware Update
- **Low Power Management**
  - Power Sleep Mode
- **Temperature Range**
  - Operation: 0°C ~ 70°C
  - Storage: -40°C ~ 85°C
- **RoHS compliant**

Notes:

1. Samples were built using Toshiba A19nm MLC “TH58TEG8DDKTA20 x 4”.
2. Please see “4.2 Power Consumption” for details.
3. Please see “TBW (Terabytes Written)” in Chapter 2 for details.

Performance and Power Consumption

Capacity	Flash Structure	Performance				Power Consumption		
		CrystalDiskMark		Test Metrix		Read (mW)	Write (mW)	Idle (mW)
		Read (MB/s)	Write (MB/s)	Read (MB/s)	Write (MB/s)			
521MB (SLC)	512MB x 1, TSOP,24nm	30	20	30	20	225	180	5
4GB	4GB x 1, TSOP,A19nm	35	10	35	10	335	250	5
8GB	4GB x 2, TSOP,A19nm	65	20	70	20	450	340	5
8GB	8GB x 1, TSOP,15nm	30	20	30	20	TBD	TBD	TBD
16GB	4GB x 4, TSOP,A19nm	105	44	110	46	670	540	5
16GB	8GB x 2,TSOP,15nm	40	40	40	40	TBD	TBD	TBD
32GB	8GB x 4, TSOP,A19nm	105	64	110	65	685	615	5
32GB	8GB x 4, TSOP,15nm	75	70	75	70	TBD	TBD	TBD
64GB	16GB x 4, TSOP,A19nm	105	80	115	80	685	910	5
64GB	16GB x 4, TSOP,15nm	70	85	75	85	TBD	TBD	TBD
128GB	32GB x 4, TSOP,A19nm	98	80	105	80	725	945	5
128GB	32GB x 4, TSOP,15nm	75	80	80	80	TBD	TBD	TBD

NOTE:

For more details on Power Consumption, please refer to Chapter 4.2.

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1. INTRODUCTION

1.1. General Description

CompactFlash™ Card is one of the most popular flash storage elements in the memory card market. By offering excellent performance and wide compatibility, Phison's CompactFlash™ Card also provides a wide range of capacities available for users. In addition, industrial-grade CompactFlash™ cards are available for any applications under rigorous environmental conditions including extensive temperature, shock and vibration.

1.2. Controller Block Diagram

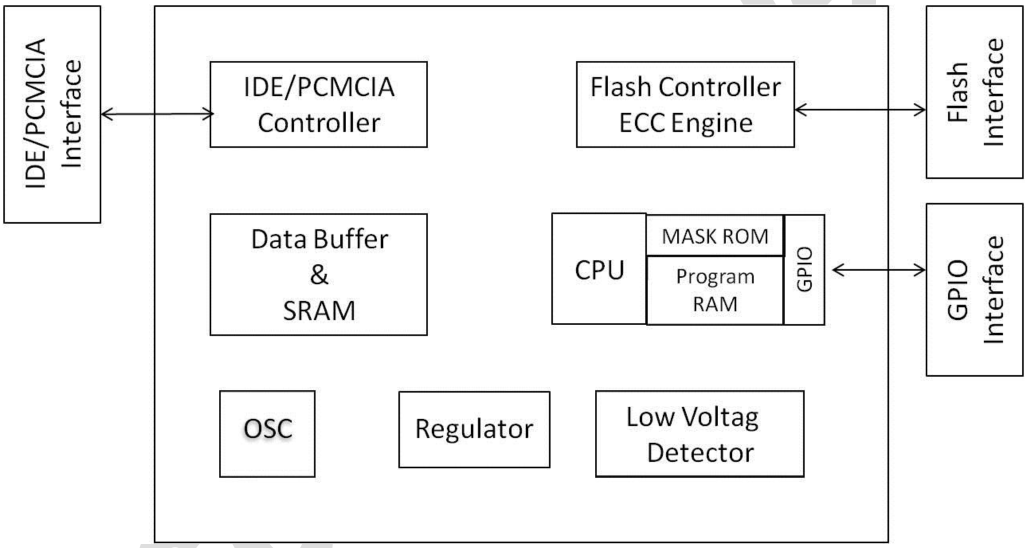


Figure 1-1 PS3016-P9 Controller Block Diagram

1.3. Product Block Diagram

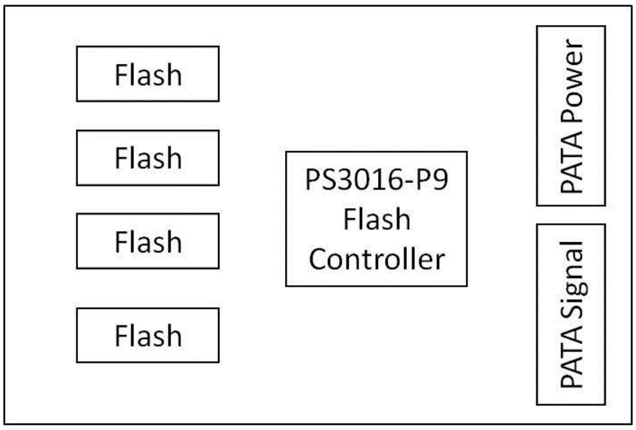


Figure 1-2 PS3016-P9 Product Block Diagram

1.4. Flash Management

1.4.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, PS3016-P9 CompactFlash™ applies the BCH ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

1.4.2. Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND flash by evenly distributing write and erase cycles across the media.

Phison provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.4.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Phison implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.4.4. Pseudo SLC (pSLC) (ultra MLC)

Pseudo SLC can be considered as an extended version of MLC. While MLC contains fast and slow pages, pSLC only applies fast pages for programming. The concept of pSLC is demonstrated in the two tables below. The first and second bits of a memory cell represent a fast and slow page respectively, as shown in the left table. Since only fast pages are programmed when applying pSLC, the bits highlighted in red are used, as shown in the right table. Accordingly, because only fast pages are programmed, pSLC provides better performance and endurance than MLC. Moreover, pSLC performs similarly with SLC, yet pSLC is more cost-effective.

MLC Flash	
1st Bit (Fast)	2nd Bit (slow)
1	1
1	0
0	1
0	0

→

Pseudo SLC Flash	
1st Bit (Fast)	2nd Bit (slow)
1	1
1	0
0	1
0	0

Figure 1-3 Cell Content of MLC (Left) and Pseudo SLC (Right)

1.4.5. Firmware Upgrade

Firmware can be considered as a set of instructions on how the device communicates with the host. Firmware will be upgraded when new features are added, compatibility issues are fixed, or read/write performance gets improved.

1.5. Power Management

Phison's CF Card provides automatic power saving modes and here are the descriptions which address the conditions and reactions when a CompactFlash card goes into a specific mode:

Standby Mode: When CF Card finishes the initialization routine after power reset, it goes into Standby Mode and will wait for Command In or Soft Reset.

Active Mode: If CF Card receives any Command In or Soft Reset, it goes into Active Mode. In Active Mode, CF card is capable of executing any ATA commands and therefore, power consumption is the greatest under this mode.

Idle Mode: After CF Card executes any ATA Commands or Soft Reset, it goes into Idle Mode. Power consumption is reduced from Active Mode.

Sleep Mode: A CF Card will enter Sleep Mode if there is no Command In or Soft Reset from the host. Sleep Mode provides the lowest power consumption. During Sleep Mode, the main clock of the system is stopped. Hardware reset, software reset or any ATA command assertion will awake the controller from Sleep Mode.

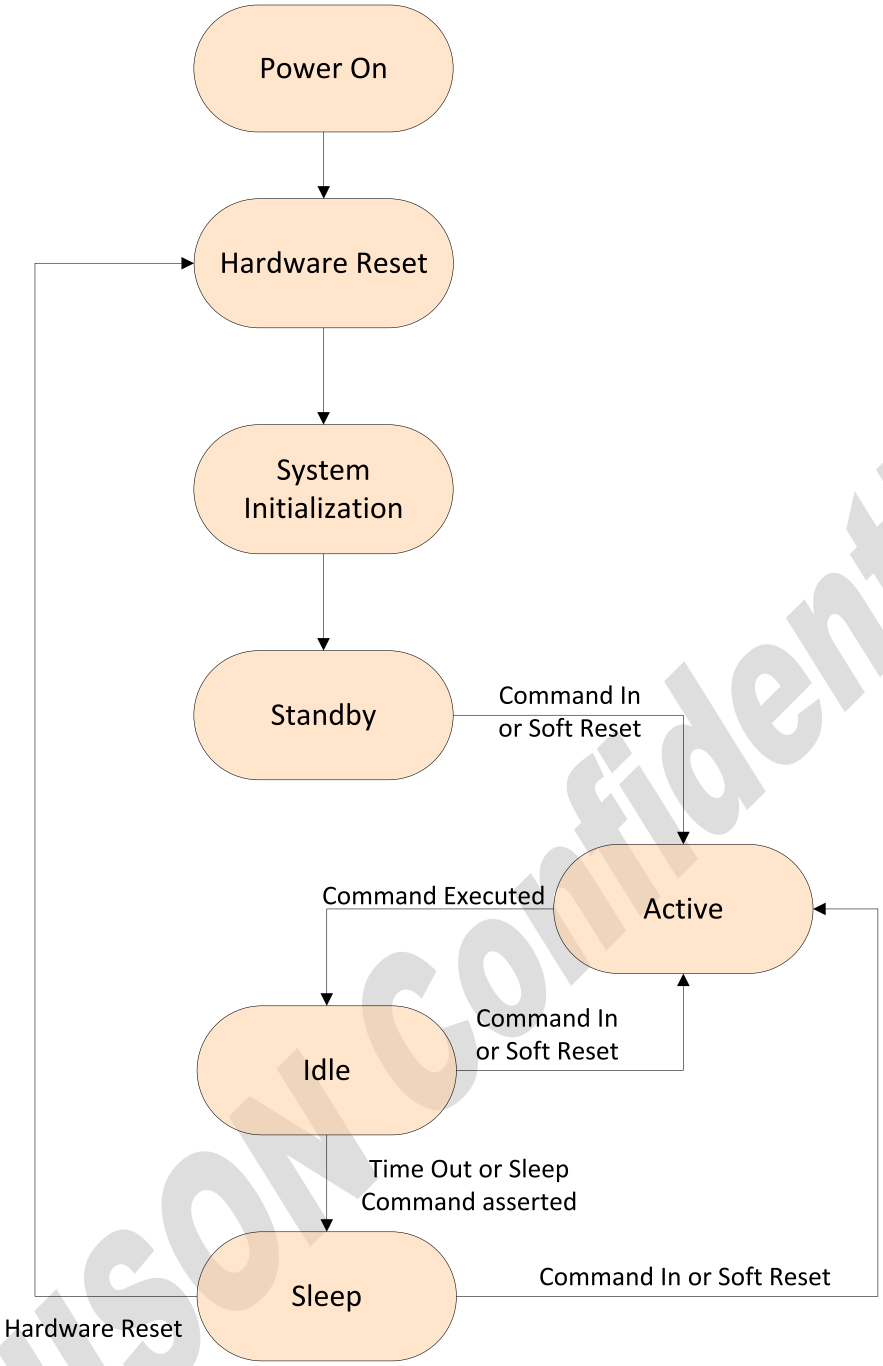


Figure 1-4 Power Saving Flow

1.6. Advanced Device Security Features

1.6.1. Secure Erase

Secure Erase is a standard ATA command and will write all "0xFF" to fully wipe all the data on hard drives and SSDs. When this command is issued, the SSD controller will erase its storage blocks and return to its factory default settings.

1.6.2. Write Protect

When a SSD contains too many bad blocks and data are continuously written in, then the SSD might not be usable anymore. Thus, Write Protect is a mechanism to prevent data from being written in and protect the accuracy of data that are already stored in the SSD.

1.7. SSD Lifetime Management

1.7.1. Terabytes Written (TBW)

TBW (Terabytes Written) is a measurement of SSDs' expected lifespan, which represents the amount of data written to the device. To calculate the TBW of a SSD, the following equation is applied:

TBW = [(NAND Endurance) x (SSD Capacity) x (WLE)] / WAF

NAND Endurance: NAND endurance refers to the P/E (Program/Erase) cycle of a NAND flash.

SSD Capacity: The SSD capacity is the specific capacity in total of a SSD.

WLE: Wear Leveling Efficiency (WLE) represents the ratio of the average amount of erases on all the blocks to the erases on any block at maximum.

WAF: Write Amplification Factor (WAF) is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near 1, guarantees better endurance and lower frequency of data written to flash memory.

2. PRODUCT SPECIFICATIONS

- **Capacity**
  - From 1GB up to 63GB for SLC flash (support 48-bit addressing mode)
  - From 4GB up to 128GB for MLC flash (support 48-bit addressing mode)
- **Supported Host Interfaces:**
  - PCMCIA/IDE Interface (support up to PIO Mode 6/Multi Word DMA Mode 4/PCMCIA Ultra DMA Mode 5/Ultra DMA Mode 7)
  - Fully compatible with CompactFlash Specification Version 3.x, 4.x, 5.x and 6.x
  - Fully compatible with PC Card Standard Release 8.0
  - Fully compatible with the IDE standard interface
  - Host Transfer Rate for PC Card/CompactFlash: 25MB/s (PIO6)
  - Host Transfer Rate for IDE standard interface: 166MB/s (UDMA7)
- **NAND Flash Interface**
  - Support SLC, MLC and Pseudo SLC NAND flash memory
  - Support 4KB/8KB/16KB data per page NAND flash memory
- **ECC Scheme**
  - PS3016-P9 CompactFlash can correct up to 68 bits error in 1K Byte data.
- **1T RISC uP8051 RAM Mode**
  - Internal RAM: 256 Bytes
  - External RAM: 24KB (On chip)
- **Support SRAM Buffer (Dual Buffer Mode):**
  - A Buffer (512 words)
  - B Buffer (512 words)
  - CIS Buffer (256 bytes)
- **Operating Voltage: 3.0 ~ 5.5V**
- **Power-saving implementation**
- **Support Static/Dynamic Wear Leveling function**
- **Support CFA VPG-20 Specification**
- **Light weight and noiseless**
- **Implemented with automatic error detection and retry capability**
- **Support power down commands and idle modes**

- **Compatible with PC card and socket services**
- **Host interface: 8/16 bit access**
- **Auto-detection of CF/ATA host interface**
- **Performance**

Capacity	Flash Structure	Flash Type	Sequential	
			Read (MB/s)	Write (MB/s)
512MB (SLC)	512MB x 1	TSOP,24nm	30	20
4GB	4GB x 1	TSOP,A19nm	35	10
8GB	4GB x 2	TSOP,A19nm	65	20
8GB	8GB x 1	TSOP,15nm	30	20
16GB	4GB x 4	TSOP,A19nm	105	44
16GB	8GB x 2	TSOP,15nm	40	40
32GB	8GB x 4	TSOP,A19nm	105	64
32GB	8GB x 4	TSOP,15nm	75	70
64GB	16GB x 4	TSOP,A19nm	105	80
64GB	16GB x 4	TSOP,15nm	70	85
128GB	32GB x 4	TSOP,A19nm	98	80
128GB	32GB x 4	TSOP,15nm	75	80

NOTES:

1. The performance was measured using CrystalDiskMark.
2. 512MB Samples was built using Toshiba 24nm SLC NAND Flash
3. Samples were built using Toshiba A19nm Toggle MLC NAND flash.
4. Performance may differ according to flash configuration, SDR configuration, and platform.
5. The table above is for reference only. The criteria for MP (mass production) and for accepting goods shall be discussed based on different flash configuration.

- **TBW (Terabytes Written)**

Capacity	Flash Structure	TBW
512MB (SLC)	512MB x 1	1
4GB	4GB x 1	2
8GB	4GB x 2	5
16GB	4GB x 4	9
32GB	8GB x 4	17
64GB	16GB x 4	34
128GB	32GB x 4	68

NOTES:

1. 4GB~128GB Samples were built using Toshiba A19nm Toggle MLC NAND flash.
2. TBW may differ according to flash configuration and platform.
3. The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor. It is not guaranteed by flash vendor.

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

- Temperature:
  - Storage: -40°C to 85°C
  - Operational: 0°C to 70°C
- Humidity: RH 90% under 40°C (operational)

Table 3-1 High Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	85°C	0% RH	72 hours
Storage	85°C	0% RH	168 hours

Result: No any abnormality is detected.

Table 3-2 Low Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	-40°C	0% RH	72 hours
Storage	-40°C	0% RH	168 hours

Result: No any abnormality is detected.

Table 3-3 High Humidity Test Condition

	Temperature	Humidity	Test Time
Operation	55°C	95% RH	72 hours
Storage	55°C	95% RH	96 hours

Result: No any abnormality is detected.

Table 3-4 Temperature Cycle Test

	Temperature	Test Time	Cycle
Operation	-40°C	30 min	20 Cycles
	85°C	30 min	
Storage	-5°C	30 min	10 Cycles
	70°C	30 min	

Result: No any abnormality is detected.

3.1.2. Shock

Table 3-5 PS3016-P9 CompactFlash™ Card Shock Specification

	Acceleration Force	Half Sin Pulse Duration
Non-operational	1500G	0.5ms

Result: No any abnormality is detected when power on.

3.1.3. Vibration

Table 3-6 PS3016-P9 CompactFlash™ Card Vibration Specification

	Condition		Vibration Orientation
	Frequency/Displacement	Frequency/Acceleration	
Non-operational	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G	X, Y, Z axis/30 min for each

Result: No any abnormality is detected when power on.

3.1.4. Drop

Table 3-7 PS3016-P9 CompactFlash™ Card Drop Specification

	Height of Drop	Number of Drop
Non-operational	110cm free fall	6 face of each unit

Result: No any abnormality is detected when power on.

3.1.5. Bending

Table 3-8 PS3016-P9 CompactFlash™ Card Bending Specification

	Force	Action
Non-operational	≥ 50N	Hold 1min/5 times

Result: No any abnormality is detected when power on.

3.1.6. Torque

Table 3-9 PS3016-P9 CompactFlash™ Card Torque Specification

	Force	Action
Non-operational	1.263N-m or 10 deg	Hold 5min/3 times

Result: No any abnormality is detected when power on.

3.1.7. Electrostatic Discharge (ESD)

Table 3-10 PS3016-P9 CompactFlash™ Card Contact ESD Specification

Device	Capacity	Temperature	Relative Humidity	+/- 4KV	Result
CompactFlash™	64GB	23.4°C	57% (RH)	Device functions are affected, but EUT will be back to its normal or operational state automatically.	PASS
	128GB				

3.1.8. EMI Compliance

- FCC: CISPR22
- CE: EN55022
- BSMI 13438

3.2. MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of Phison's PS3016-P9 CompactFlash™ Card is more than 1,000,000 hours.

3.3. Certification & Compliance

- RoHS
- CompactFlash Specification Version 6.0
- Up to ATA/ATAPI-8 (Including S.M.A.R.T)

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage

Table 4-1 Supply Voltage of PS3016-P9 CompactFlash Card

Parameter	Rating
Operating Voltage	3.3V and 5.0V

4.2. Power Consumption

Table 4-2 Power Consumption of PS3016-P9 CompactFlash Card

Capacity	Flash Structure	Read	Write	Idle
512MB	512MB x 1,24nm	225	180	5
4GB	4GB x 1,A19nm	335	250	5
8GB	4GB x 2,A19nm	450	340	5
8GB	8GB x 1,15nm	TBD	TBD	TBD
16GB	4GB x 4,A19nm	670	540	5
16GB	8GB x 2,15nm	TBD	TBD	TBD
32GB	8GB x 4,A19nm	685	615	5
32GB	8GB x 4,15nm	TBD	TBD	TBD
64GB	16GB x 4,A19nm	685	910	5
64GB	16GB x 4,15nm	TBD	TBD	TBD
128GB	32GB x 4 A19nm	725	945	5
128GB	32GB x 4 15nm	TBD	TBD	TBD

Unit: mW

NOTES:

1. Samples was build using Toshiba 24nm SLC for 512MB
2. Samples were built using Toshiba A19nm Toggle MLC NAND flash for 4GB~1280GB.
3. The operating voltage is 3.3V.
4. Sequential R/W is measured while testing 4000MB sequential R/W 5 times by CyrstalDiskMark.
5. Power Consumption may vary from flash configuration or platform.

4.3. Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit	Remark
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+5.5	V	
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V	
3	Ta	Operating Temperature	0	+70	°C	Commercial Grade
4	Tst	Storage Temperature	-25	+85	°C	Commercial Grade
5	Ta	Operating Temperature	-40	+85	°C	Industrial Grade

6	Tst	Storage Temperature	-40	+85	°C	Industrial Grade

Parameter	Symbol	Min	TYP	MAX	Unit
V_{DD} Voltage	V_{DD}	3.0	3.3	3.6	V
		4.5	5.0	5.5	V

4.4. DC Characteristics

Table 4-3 DC Characteristics of 5.0V I/O Cells (Host Interface)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Vol	Output Low voltage	|Iol| = 4 ~ 32 mA	-	-	0.4	V
Voh	Output High voltage	|Ioh| =4 ~ 32 mA	2.4	-	-	V
Rpu	Input Pull-Up Resistance	PU=high, PD=low	200	300	450	KΩ
Rpd	Input Pull-Down Resistance	PU=high, PD=low	200	300	450	KΩ
Iin	Input Leakage Current	Vin = VCC3I or 0	-10	±1	10	μA
Ioz	Tri-state Output Leakage Current		-10	±1	10	μA

4.5. AC Characteristics

4.5.1. PCMCIA Interface

Attribute Memory Read Timing

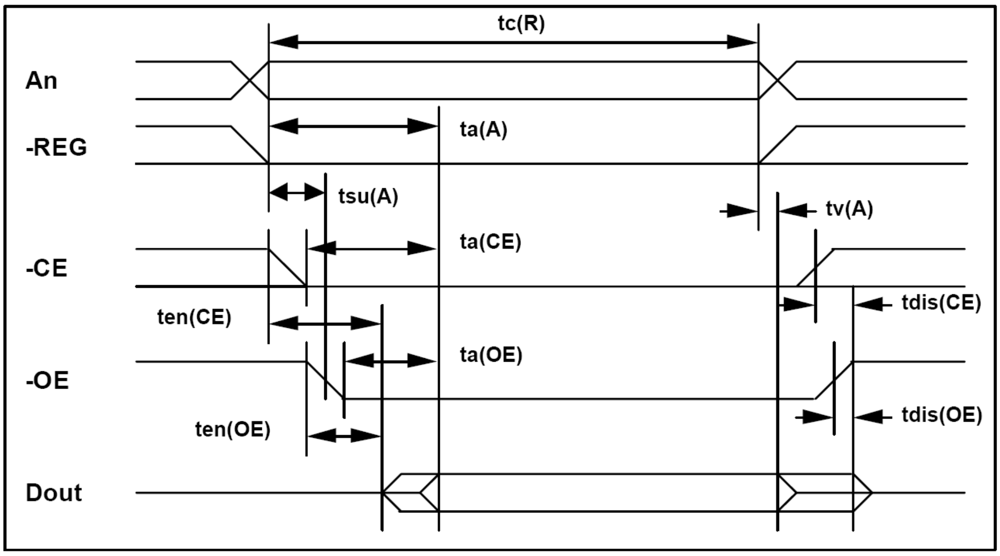


Figure 4-1 Attribute Memory Read Timing

Table 4-4 Attribute Memory Read Timing

Speed Version	Symbol	IEEE Symbol	300 ns.	
Item			Min ns.	Max ns.
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(a)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVGL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

Attribute Memory Write Timing

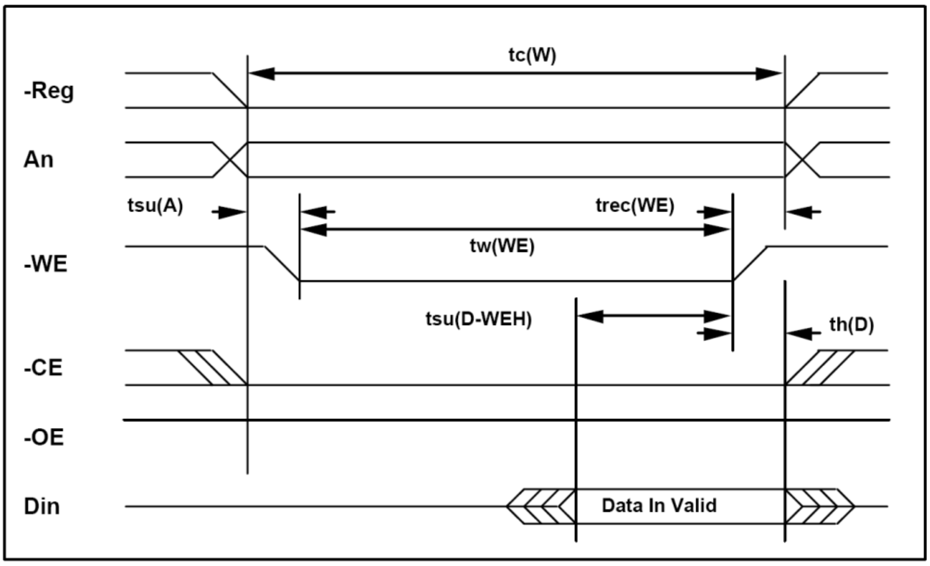


Figure 4-2 Attribute Memory Write Timing

Table 4-5 Attribute Memory Writing Timing

Speed Version	Symbol	IEEE Symbol	250 ns	
Item			Min ns	Max ns
Write Cycle Time	tc(W)	tAVAV	250	

Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

Common Memory Read Timing

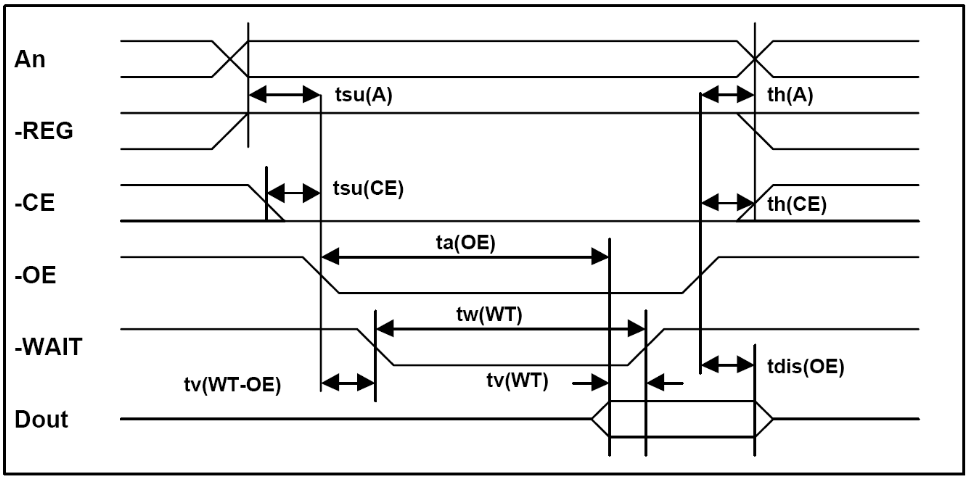


Figure 4-3 Common Memory Read Timing

Table 4-6 Common Memory Read Timing

Cycle Time Mode			**250 ns**		**120 ns**		**100 ns**		**80 ns**	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from	tv(WT-OE)	tGLWTV		35		35		35		na[1]

OE										
Data Setup for Wait Release	tv(WT)	tQVWTH		0		0		0		na[1]
Wait Width Time[2]	tw(WT)	tWTLWTH		350(3000 for CF+)		350(3000 for CF+)		350(3000 for CF+)		na[1]

NOTES:

1. -WAIT is not supported in this mode.
2. The maximum load on –WAIT is 1 LSTTL with 50pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The –WAIT signal may be ignored if the –OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12us but is intentionally less in this specification.

Common Memory Write Timing

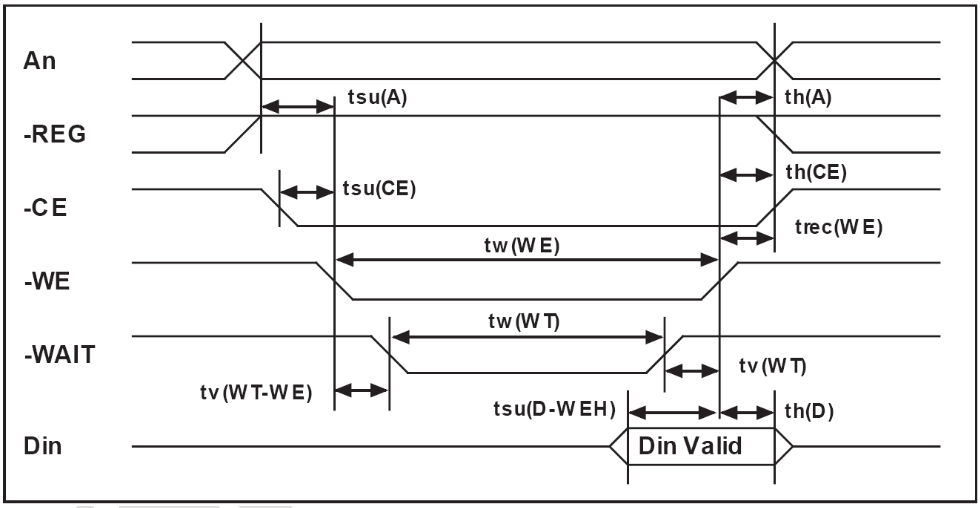


Figure 4-4 Common Memory Write Timing

Table 4-7 Common Memory Write Timing

Cycle Time Mode			250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before WE	tsu(D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tWMDX	30		15		10		10	
WE Pulse	tw(WE)	tWLWH	150		70		60		55	

Width										
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	

Cycle Time Mode			**250 ns**		**120 ns**		**100 ns**		**80 ns**	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		15	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV		35		35				na[1]
WE High from Wait Release	tv(WT)	tWTHWH	0		0		0		na[1]	
Wait Width Time[2]	tw(WT)	tWTLWTH		350(3000 for CF+)		350(3000 for CF+)		350(3000 for CF+)		na[1]

NOTES:

1. –WAIT is not supported in this mode.
2. The maximum load on –WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The –WAIT signal may be ignored if the –WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12us but is intentionally less in this specification.

I/O Read Timing

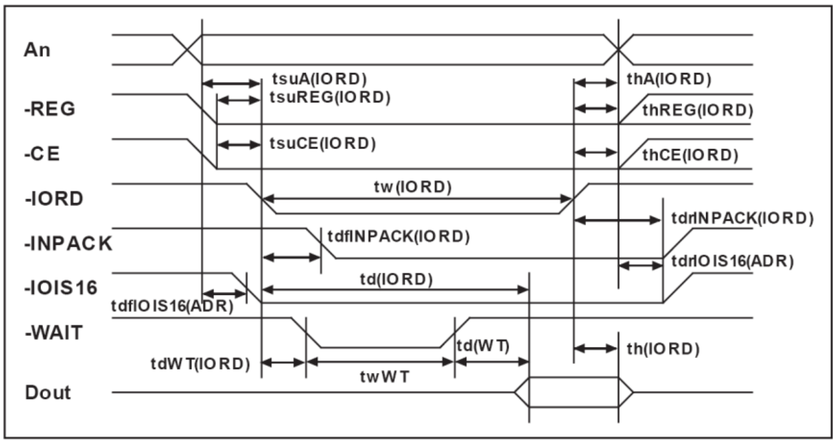


Figure 4-5 I/O Read Timing

Table 4-8 I/O Read Timing

Cycle Time Mode			250 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min (ns.)	Max (ns.)	Min (ns.)	Max (ns.)	Min (ns.)	Max (ns.)	Min (ns.)	Max (ns.)
Data Delay after IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tIGHQX	0		5		5		5	
IORD W idth Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10		10		10	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10		10		10	
REG Setup before IORD	tsuREG (IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG (IORD)	tIGHRGH	0		0		0		0	
INPACK Delay Falling from IORD[3]	tdfINPACK (IORD)	tIGLIAL	0	45	0	na[1]	0	na[1]	0	na[1]
INPACK Delay Rising from IORD[3]	tdrINPACK (IORD)	tIGHIAH		45		na[1]		na[1]		na[1]
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]

Wait Delay Falling from IORD[3]	tdW T(IORD)	tIGLW TL		35		35		35		na[2]
Data Delay from Wait Rising[3]	td(W T)	tW THQV		0		0		0		na[2]
Wait Width Time[3]	tw(W T)	tW TLW TH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[2]

NOTES:

1. -IOIS16 and -INPACK are not supported in this mode.
2. -WAIT is not supported in this mode.
3. Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA PC Card specification of 12µs but is intentionally less in this spec.

I/O Write Timing

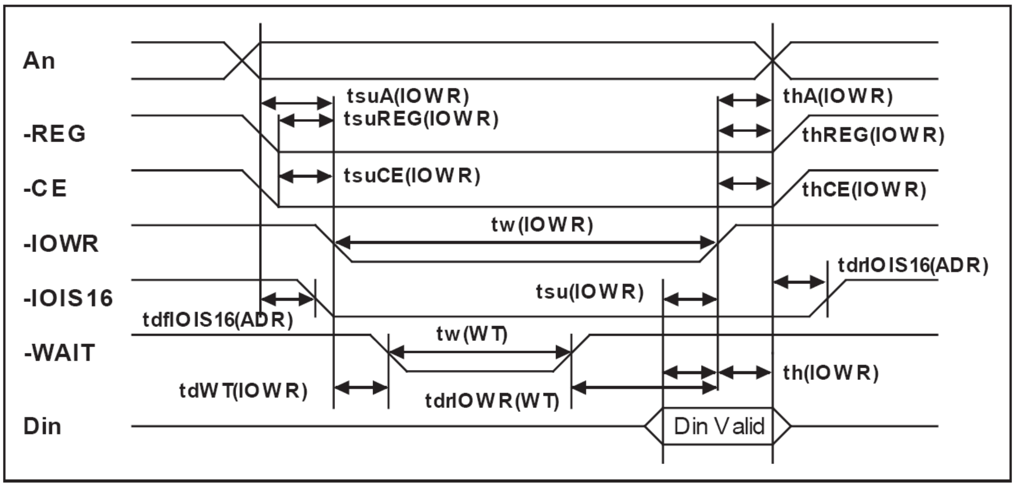


Figure 4-6 I/O Write Timing

Table 4-9 I/O Write Timing

Cycle Time Mode			255 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min (ns.)**	**Max (ns.)**	**Min (ns.)**	**Max (ns.)**	**Min (ns.)**	**Max (ns.)**	**Min (ns.)**	**Max (ns.)**
Data Setup before IOWR	tsu(IOW R)	tDVIW H	60		20		20		15	
Data Hold following IOWR	th(IOW R)	tIWHDX	30		10		5		5	

IOW R Width Time	tw(IOW R)	tIWLIW H	165		70		65		55	
Address Setup before IOW R	tsuA(IOW R)	tAVIW L	70		25		25		15	
Address Hold following IOW R	thA(IOW R)	tIWHAX	20		20		10		10	
CE Setup before IOWR	tsuCE (IOW R)	tELIW L	5		5		5		5	
CE Hold following IOWR	thCE (IOW R)	tIWHEH	20		20		10		10	
REG Setup before IOWR	tsuREG (IOW R)	tRGLIW L	5		5		5		5	
Cycle Time Mode			**255 ns**		**120 ns**		**100 ns**		**80 ns**	
Item	**Symbol**	**IEEE Symbol**	**Min (ns.)**	**Max (ns.)**	**Min (ns.)**	**Max (ns.)**	**Min (ns.)**	**Max (ns.)**	**Min (ns.)**	**Max (ns.)**
REG Hold following IOWR	thREG (IOW R)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IOW R[3]	tdW T (IOWR)	tIWLW TL		35		35		35		na[2]
IOW R high from Wait High[3]	tdrIOW R (W T)	tW TJIWH	0		0		0		na[2]	
Wait Width Time[3]	Tw (W T)	tW TLW TH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[2]

NOTES:

1. -IOIS16 and -INPACK are not supported in this mode.
2. -WAIT is not supported in this mode.
3. The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0nsec, but minimum -IOW R width shall still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA PC Card specification of 12 µs but is intentionally less in this specification.

4.5.2. IDE Interface Timing (PIO Mode)

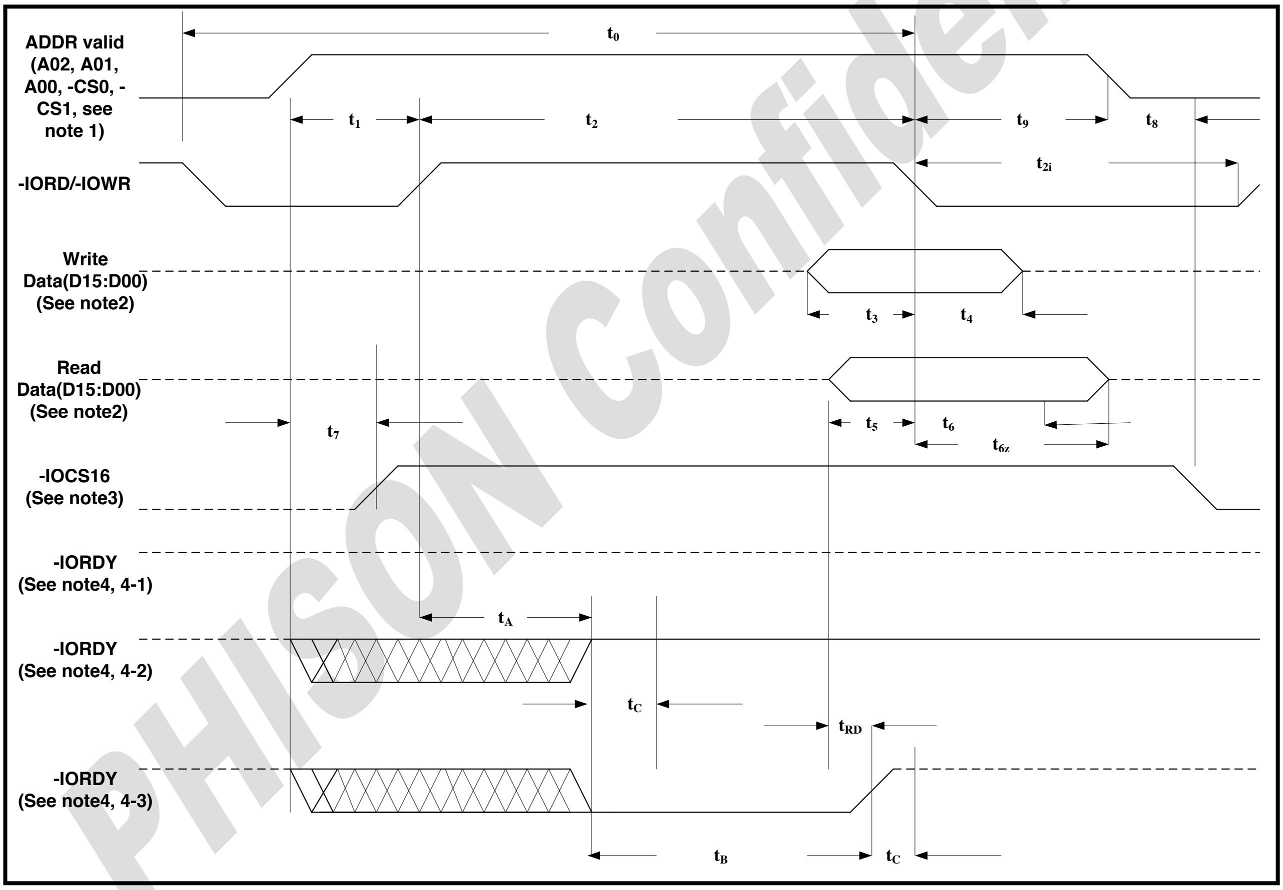


Figure 4-7 IDE Interface Timing (PIO Mode)

NOTES:

1. Device address consists of -CS0, -CS1, and A[02:00]
2. Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
3. -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
4. The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The

assertion and negation of IORDY is described in the following three cases:

- Device never negates IORDY: No wait is generated.
- Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
- Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

Table 4-10 IDE Interface Timing

Name	Item	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Note
t0	Cycle time (min)	600	383	240	180	120	100	80	1
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	15	10	
t2	-IORD/-IOWR (min)	165	125	100	80	70	65	55	1
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	65	55	1
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	25	20	1
t3	-IOWR data setup (min)	60	45	30	30	20	20	15	
t4	-IOWR data ho ld (min)	30	20	15	10	10	5	5	
t5	-IORD data setup (min)	50	35	20	20	20	15	10	
t6	-IORD data hold (min)	5	5	5	5	5	5	5	
T6Z	-IORD data tristate (max)	30	30	30	30	30	20	20	2
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a	4
t8	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a	4
t9	-IORD/-IOWR to address valid ho ld	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially lo w after tA	0	0	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	na5	na5	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na5	na5	

tC	IORDY assertion to release (max)	5	5	5	5	5	na5	na5	

NOTES:

All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0nsec, but minimum -IORD width shall still be met.

1. t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.
2. This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).
3. The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the CompactFlash Storage Card is driving IORDY negated at the time tA after the activation of -IORD or -IOW R, then tRD shall be met and t5 is not applicable.
4. t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.
5. IORDY is not supported in this mode.

4.5.3. Multi Word DMA

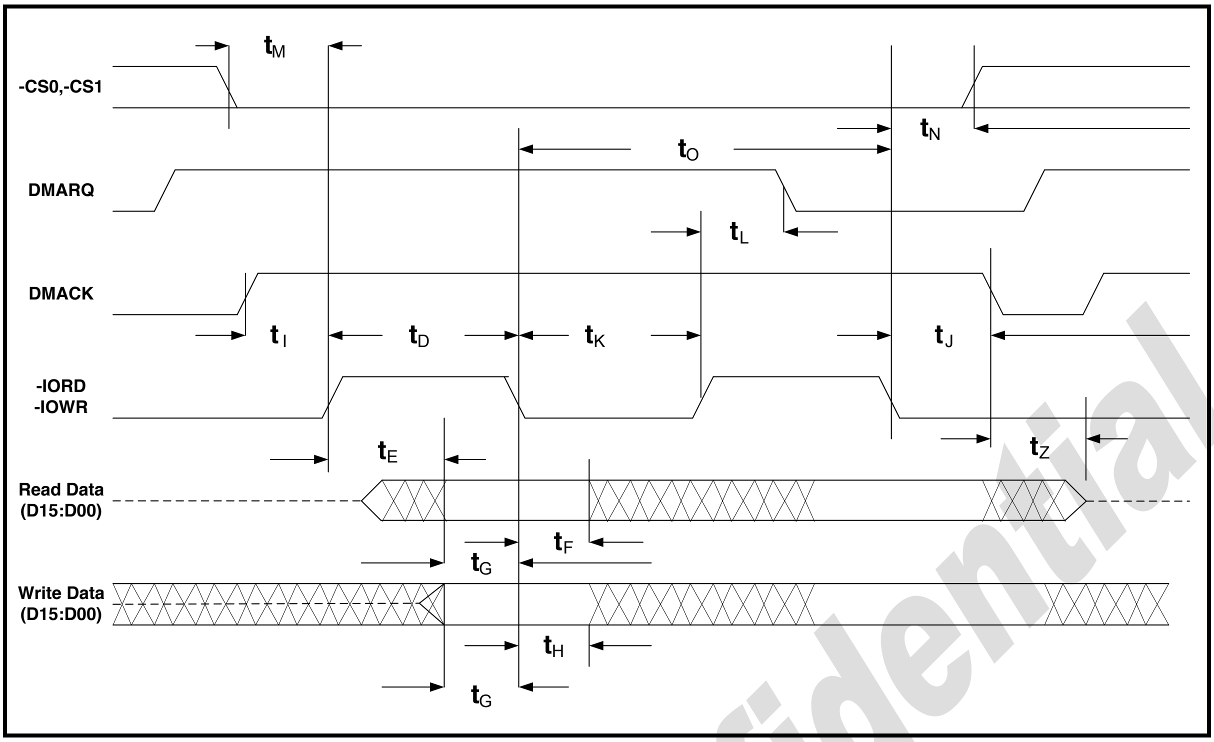


Figure 4-8 Multi Word DMA

NOTES:

All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

1. If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.
2. This signal may be negated by the host to suspend the DMA transfer in progress.

Table 4-11 MDMA Mode Timing Table

Item		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note
	Symbol	(ns)	(ns)	(ns)	(ns)	(ns)	
t_0	Cycle time (min)	480	150	120	100	80	1
t_D	-IORD / -IOWR asserted width (min)	215	80	70	65	55	1
t_E	-IORD data access (max)	150	60	50	50	45	
t_F	-IORD data hold (min)	5	5	5	5	5	
t_G	-IORD / -IOWR data setup (min)	100	30	20	15	10	
t_H	-IOWR data hold (min)	20	15	10	5	5	
t_I	DMACK to -IORD/-IOWR setup	0	0	0	0	0	

	(min)						
t_J	-IORD / -IOWR to -DMACK hold (min)	20	5	5	5	5	
t_{KR}	-IORD negated width (min)	50	50	25	25	20	1
t_{KW}	-IOWR negated width (min)	215	50	25	25	20	1
t_{LR}	-IOWR to DMARQ delay (max)	120	40	35	35	35	
t_{LW}	-IOWR to DMARQ delay (max)	40	40	35	35	35	
t_M	CS(1:0) valid to -IORD/-IOWR	50	30	25	10	5	
t_N	CS(1:0) hold	15	10	10	10	10	
t_Z	-DMACK	20	25	25	25	25	

NOTE:

1. t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_D, t_{KR} and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D, t_{KR} and t_{KW} for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR} and t_{KW} as needed to ensure that t_D is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

4.5.4. Ultra DMA

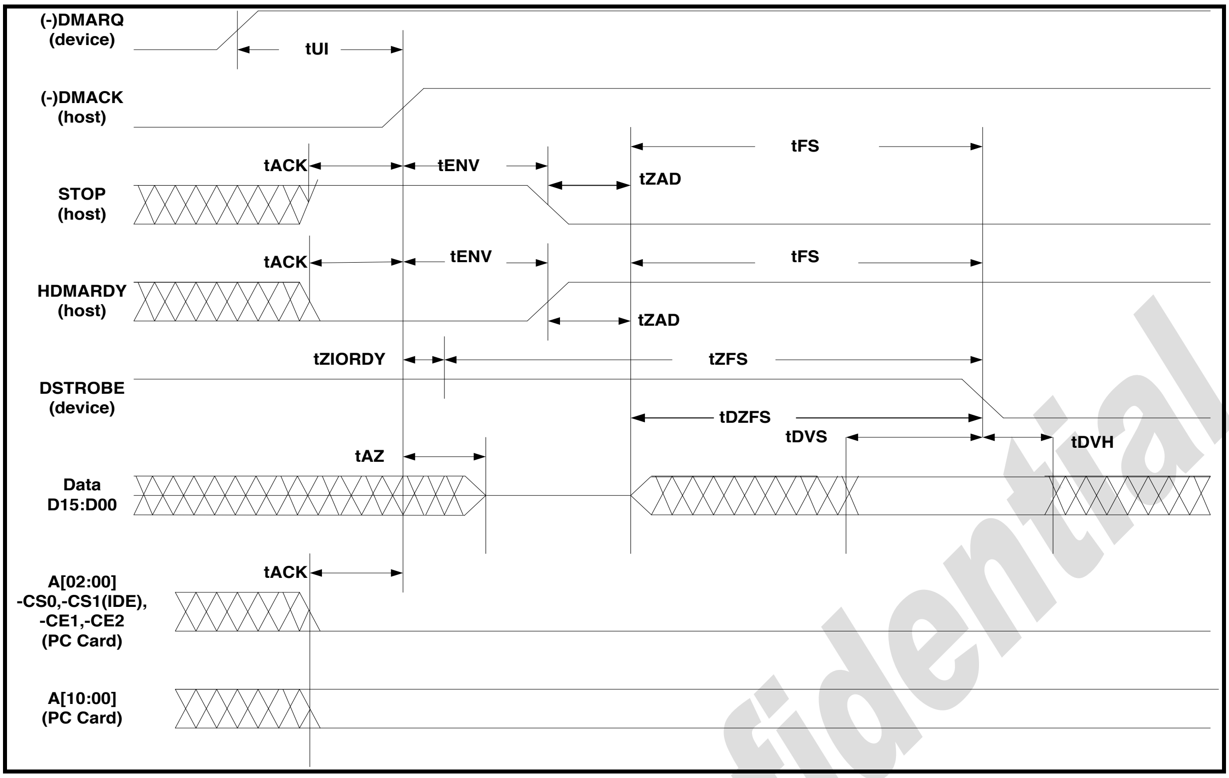


Figure 4-9 Initialize an Ultra DMA Data in Burst Timing

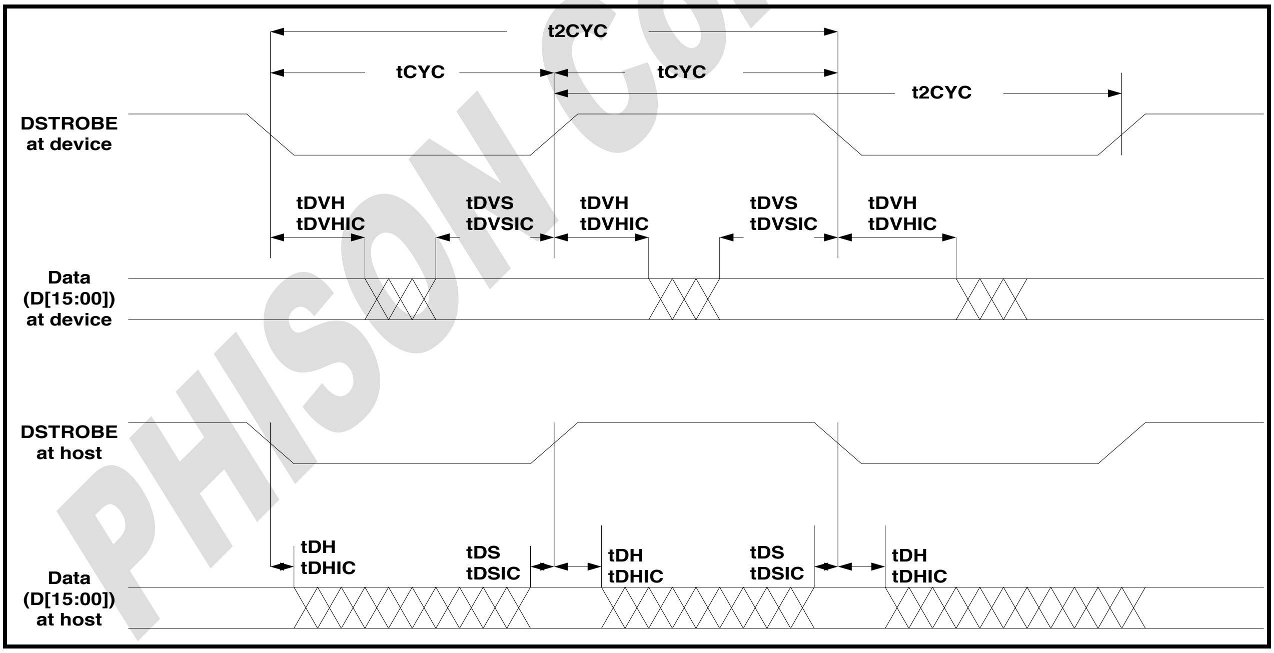


Figure 4-10 Sustained Ultra DMA Data-in Burst Timing

Table 4-12 Ultra DMA Mode Timing

	UDMA																Measure
Name	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Mode 6		Mode7		Location
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	(See Note 2)
t2CYCTYP	240		160		120		90		60		40		30		24		Sender
tCYC	112		73		54		39		25		16.8		13		10		Note 3
t2CYC	230		153		115		86		57		38		29		23		Sender
tDS	15		10		7		7		5		4		2.6		2.5		Recipient
tDH	5		5		5		5		5		4.6		3.5		2.9		Recipient
tDVS	70		48		31		20		6.7		4.8		4		2.9		Sender
tDVH	6.2		6.2		6.2		6.2		6.2		4.8		4		3.2		Sender
tCS	15		10		7		7		5		5		5		5		Device
tCH	5		5		5		5		5		5		5		5		Device
tCVS	70		48		31		20		6.7		10		10		10		Host
tCVH	6.2		6.2		6.2		6.2		6.2		10		10		10		Host
tZFS	0		0		0		0		0		35		25		15		Device
tDZFS	70		48		31		20		6.7		25		17.5		10.5		Sender
tFS		230		200		170		130		120		90		80		70	Device
tLI	0	150	0	150	0	150	0	100	0	100	0	75	0	60	0	50	Note 4
tMLI	20		20		20		20		20		20		20		20		Host
tUI	0		0		0		0		0		0		0		0		Host
tAZ		10		10		10		10		10		10		10		10	Note 5
tZAH	20		20		20		20		20		20		20		20		Host
tZAD	0		0		0		0		0		0		0		0		Device
tENV	20	70	20	70	20	70	20	55	20	55	20	50	20	50	20	50	Host
tRFS		75		70		60		60		60		50		50		50	Sender
tRP	160		125		100		100		100		85		85		85		Recipient
tIORDYZ		20		20		20		20		20		20		20		20	Device
tZI ORDY	0		0		0		0		0		0		0		0		Device
tACK	20		20		20		20		20		20		20		20		Host
tSS	50		50		50		50		50		50		50		50		Sender

Table 4-13 Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
t2CYCTYP	Typical sustained average two cycle time	
tCYC	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t2CYC	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
tDS	Data setup time at recipient (from data valid until STROBE edge)	2, 5
tDH	Data ho ld time at recipient (from STROBE edge until data may become invalid)	2, 5
tDVS	Data valid setup time at sender (from data valid until STROBE edge)	3
tDVH	Data valid ho ld time at sender (from STROBE edge until data may become invalid)	3
tCS	CRC word setup time at device	2
tCH	CRC word hold time device	2
tCVS	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
tCVH	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
tZFS	Time from STROBE output released-to-driving until the first transition of critical timing.	
tDZFS	Time from data output released-to-driving until the first transition of critical timing.	
tFS	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
tLI	Limited interlock time	1
tMLI	Interlock time with minimum	1
tUI	Unlimited interlock time	1
tAZ	Maximum time allowed for output drivers to release (from asserted or negated)	
tZAH	Minimum delay time required for output	
tZAD	drivers to assert or negate (from released)	
tENV	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK	
	to STOP during data out burst initiation)	
tRFS	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
tRP	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
tIORDYZ	Maximum time before releasing IORDY	6
Name	**Comment**	**Notes**

t_{ZIORDY}	Minimum time before driving IORDY	4, 6
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

NOTES:

1. The parameters t_{UI}, t_{MLI}, and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.
2. 80-conductor cabling shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.
3. Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
4. For all timing modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.
5. The parameters t_{DS} and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.
6. This parameter applies to True IDE mode operation only.

5. INTERFACE

5.1. Pin Assignment and Descriptions

Table 5-1 CompactFlash™ Interface Pin Assignments

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin #	Signal Name	Pin Type	Pin #	Signal Name	Pin Type	Pin #	Signal Name	Pin Type
1	GND		1	GND		1	GND	
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	-CE1	I	7	-CE1	I	7	-CSO	I
8	A10	I	8	A10	I	8	A10	I
9	-OE	I	9	-OE	I	9	-ATA SEL	I
10	A09	I	10	A09	I	10	A09	I
11	A08	I	11	A08	I	11	A08	I
12	A07	I	12	A07	I	12	A07	I
13	VCC		13	VCC		13	VCC	I
14	A06	I	14	A06	I	14	A06	I
15	A05	I	15	A05	I	15	A05	I
16	A04	I	16	A04	I	16	A04	I
17	A03	I	17	A03	I	17	A03	I
18	A02	I	18	A02	I	18	A02	I
19	A01	I	19	A01	I	19	A01	I
20	A00	I	20	A00	I	20	A00	I/O
21	D00	I/O	21	D00	I/O	21	D00	I/O
22	D01	I/O	22	D01	I/O	22	D01	I/O
23	D02	I/O	23	D02	I/O	23	D02	I/O
24	WP	O	24	-IOIS16	O	24	-IOIS16	O
25	-CD2	O	25	-CD2	O	25	-CD2	O
26	-CD1	O	26	-CD1	O	26	-CD1	O
27	D11	I/O	27	D11	I/O	27	D11	I/O
28	D12	I/O	28	D12	I/O	28	D12	I/O
29	D13	I/O	29	D13	I/O	29	D13	I/O
30	D14	I/O	30	D14	I/O	30	D14	I/O
31	D15	I/O	31	D15	I/O	31	D15	I

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin #	Signal Name	Pin Type	Pin #	Signal Name	Pin Type	Pin #	Signal Name	Pin Type
32	-CE2	I	32	-CE2	I	32	-CS1	O
33	-VS1	O	33	-VS1	O	33	-VS1	I
34	-IORD	I	34	-IORD	I	34	-IORD	I
35	-IOWR	I	35	-IOWR	I	35	-IOWR	I
36	-WE	I	36	-WE	I	36	-WE	I
37	RDY/BSY	O	37	IREQ	O	37	INTRQ	
38	VCC		38	VCC		38	VCC	I
39	-CSEL	I	39	-CSEL	I	39	-CSEL	I
40	-VS2	O	40	-VS2	O	40	-VS2	I
41	RESET	I	41	RESET	I	41	RESET	O
42	-WAIT	O	42	-WAIT	O	42	IORDY	O
43	-INPACK	O	43	-INPACK	O	43	DMARQ	I
44	-REG	I	44	-REG	I	44	DMACK	I/O
45	BVD2	I/O	45	-SPKR	I/O	45	-DASP	I/O
46	BVD1	I/O	46	-STSCHG	I/O	46	-PDIAG	I/O
47	D08	I/O	47	D08	I/O	47	D08	I/O
48	D09	I/O	48	D09	I/O	48	D09	I/O
49	D10	I/O	49	D10	I/O	49	D10	
50	GND		50	GND		50	GND	

NOTES:

1. WE should be connected to VCC in True IDE mode.

2. CSEL is the input pin for master/slave selection used in True IDE mode.

Table 5-2 Power Segment Pin Assignment and Descriptions

Signal Name	Dir.	Pin	Description
BVD2 (PC Card Memory Mode)	I/O	45	This output line is always driven to a high state in Memory Mode since a battery is not required for this product
-SPKR (PC CARD I/O Mode)			This output line is always driven to a high state in I/O Mode since this product does not support the audio function
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol
-CD1,-CD2 (PC Card Memory Mode)	O	26, 25	These card detect pins are connected to the ground on the CompactFlash™ Storage Card. They are used by the host to determine that the CompactFlash™ Storage Card is fully inserted into its socket.
-CD1,-CD2 (PC Card I/O Mode)			The signal is the same for all modes
-CD1,-CD2 (True IDE Mode)			The signal is the same for all modes
D[15:0] (PC Card Memory Mode)	I/O	31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21	These lines carry the Data, Commands, and Status information between the host and the controller. D00 is the LSB of the Odd Byte of the World
D[15:0] (PC Card I/O Mode)			The signal is the same as the PC Card Memory Mode signal.
D[15:0] (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the lower order bus D00-D07 while all data transfers are 16 bit using D00-D15.
-IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash™ Storage Card or CF+ Card controller registers when the CompactFlash™ Storage Card or CF+ Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
STOP (True IDE Mode – Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
-IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.

Signal Name	Dir.	Pin	Description
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash™ Storage Card or CF+ Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.
-HDMARDY (True IDE Mode – In Ultra DMA Protocol DMA Read)			In True IDE Mode when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in burst. The host may negate –HDMARDY to pause an Ultra DMA transfer.
-HSTROBE (True IDE Mode – In Ultra DMA Protocol DMA Write)			In True IDE Mode when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
-WE (PC Card Memory Mode)	I	36	This signal is driven by the host and used for strobing memory write data to the registers of the CompactFlash™ Storage Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.
-OE (PC Card Memory Mode)	I	9	This is an Ouput Enable strobe generated by the host interface. It is used to read data from the CompactFlash™ Storage Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode this input, this signal is used to read the CIS and configuration registers.
-OE (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
RDY/-BSY (PC Card Memory Mode)	O	37	In Memory Mode this signal is set high when the CompactFlash™ Storage Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY is held low (busy) until the CompactFlash™ Storage Card has completed its power up or reset function. No access of any type should be made to the CompactFlash™ Storage Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The CompactFlash™ Storage Card has been powered up with +RESET continuously disconnected or asserted.

Signal Name	Dir.	Pin	Description
-IREQ (PC Card I/O Mode)			I/O Operation- After the CompactFlash™ Storage has been configured for I/O operation, this signal is used as – Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is an active high Interrupt Request to the host.
A[10:0] (PC Card Memory Mode)	I	8, 10, 11, 12, 14, 15, 16, 17, 18, 19, 20	These address lines along with the –REG signal are used to select the following: The I/O port address registers within the CompactFlash™ Storage Card, the memory mapped port address registers within the CompactFlash™ Storage Card, a byte in the card's information structure and its configuration control and status registers.
A[10:0] (PC Card I/O Mode)			The signal is the same as the PC Card Memory Mode signal.
A[2:0] (True IDE Mode)			In True IDE Mode only HA[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host .
-CE1,-CE2 (PC Card Memory Mode) Card Enable	I	7, 32	These input signals are used to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on the A0 and –CE2. A multi-plexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7.
-CE1,-CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0,-CS1 (True IDE Mode)			In the True IDE Mode CS0 is the chip select for the task file registers while CS2 is used to select the Alternate Status Register and the Device Control Register.
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
-REG (PC Card Memory Mode) Attribute Memory Select	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory
-REG (PC Card I/O Mode)			The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.

Signal Name	Dir.	Pin	Description
-DMACK (True IDE Mode)			This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore -DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
WP (PC Card Memory Mode) Write Protect			Memory Mode- The CompactFlash™ Storage Card does not have a write protect switch. This signal is held low after the addressed port.
-IOIS 16 (PC Card I/O Mode)	O	24	I/O Operation- When the CompactFlash™ Storage Card is configured for I/O Operation Pin 24 is used for the –I/O Selected is a 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOIS 16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.
-VS1 **-VS2** (PC Card Memory Mode)			Voltage Sense Signals. –VS1 is grounded so that the CompactFlash™ Storage Card CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage.
-VS1 **-VS2** (PC Card I/O Mode)	O	33 40	This signal is the same for all modes.
-VS1 **-VS2** (True IDE Mode)			This signal is the same for all modes.
-INPACK (PC Card Memory Mode)			This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge	O	43	The Input Acknowledge signal is asserted by the CompactFlash™ Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between CompactFlash™ Storage Card or CF+ Card and the CPU.

Signal Name	Dir.	Pin	Description
-DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by –IORD and –IOWR. This signal is used in a handshake manner with –DMACK, ie: the device shall wait until the host asserts –DMACK before negating DMARQ, and re-asserting DMARQ if there is more data to transfer. DMARQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.
BVD1 (PC Card Memory Mode)			This signal is asserted high as the BVD1 signal since a battery is not used with this product.
-STSCHG (PC Card I/O Mode) Status Changed	I/O	46	This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
-WAIT (PC Card Memory Mode)			The –WAIT signal is driven low by the CompactFlash™ Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode – Except Ultra DMA Mode)	O	42	In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.
-DDMARDY (True IDE Mode – Ultra DMA Write Mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is ready to receive Ultra DMA data-in bursts. The device may negate –DDMARDY to pause an Ultra DMA transfer.

Signal Name	Dir.	Pin	Description
-DSTROBE (True IDE Mode – Ultra DMA Read Mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
GND (PC Card Memory Mode)	--	1, 50	Ground.
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.
VCC (PC Card Memory Mode)	--	13, 38	+5V, +3.3V power
VCC (PC Card I/O Mode)			This signal is the same for all modes.
VCC (True IDE Mode)			This signal is the same for all modes.
RESET (PC Card Memory Mode)	I	41	When the pin is high this signal Resets the CompactFlash™ Storage Card. The CompactFlash™ Storage Card is Reset only at power up if this pin is left high or open from power up. The CompactFlash™ Storage Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			The signal is the same as the PC Card Memory Mode signal.
RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.

Table 5-3 LBA and CHS Parameters per Capacity

Capacity	LBA	CHS		
		Cylinders	Head	Sector
1GB	1,951,488	1936	16	63
2GB	3,902,976	3872	16	63
4GB	7,806,960	7745	16	63
8GB	15,613,920	15490	16	63
16GB	31,227,840	16383	16	63
32GB	62,586,720	16383	16	63
64GB	126,090,720	16383	16	63
128GB	252,182,448	16383	16	63

6. SUPPORTED COMMANDS

6.1. Identify Drive Information

Table 6-1 List of Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848AH	2	General configuration bit-significant information
1	XXXX	2	Default number of cylinders
2	0000H	2	Reserved
3	XXXX	2	Default number of heads
4	0000H	2	Retired
5	0200H	2	Retired
6	XXXX	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card
9	0000H	2	Retired
10-19	XXXX	20	Serial Number in ASCII
20	0002H	2	Retired
21	0002H	2	Retired
22	0004H	2	Obsolete
23-26	XXXX	8	Firmware revision in ASCII
27-46	XXXX	40	Model number in ASCII
47	0001H	2	Maximum number of sector that shall be transferred on Read/Write Multiple commands
48	0000H	2	Reserved
49	0300H	2	Obsolete
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode 2
52	0000H	2	Retired
53	0007H	2	Word 54-58, 64-70 and 88 are valid
54	XXXX	2	Current numbers of cylinders
55	XXXX	2	Current numbers of heads
56	XXXX	2	Current sectors per track
57-58	XXXX	4	Current capacity in sectors (LBAs)(Word 57= LSW, Word 58= MSW)
59	0101H	2	Multiple sector setting is valid
60-61	XXXX	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Retired
63	0007H	2	Multiword DMA mode 2 and below are supported
64	0003H	2	Advance PIO transfer modes supported

Word Address	Default Value	Total Bytes	Data Field Type Information
65	0078H	2	Minimum Multiword DMA transfer cycle time 120nsec
66	0078H	2	Manufacturer's recommended Multiword DMA transfer cycle time 120nsec
67	0078H	2	Minimum PIO transfer cycle time without flow control 120nsec
68	0078H	2	Minimum PIO transfer cycle time with IORDY flow control 120nsec
69-81	0000H	26	Reserved
82	0002H	2	Supports Security Mode feature set
83-87	0000H	10	Reserved
88	0X3FH	2	Ultra DMA mode 5 and below are supported
89-127	0000H	78	Reserved
128	0021H	2	Enhanced security erase supported
129-159	0000H	62	Reserved vendor unique bytes
160-255	0000H	192	Reserved

6.2. CIS Information

Table 6-2 CIS Information

Address	Data	Description of Contents	CIS Function
000H	01H	CISTPL_DEVICE	Tuple code
002H	04H	TPL_LINK	Tuple link
004H	DFH	Device information	Tuple data
006H	4AH	Device information	Tuple data
008H	01H	Device information	Tuple data
00AH	FFH	END MARKER	End of Tuple
00CH	1CH	CISTPL_DEVICE_OC	Tuple code
00EH	04H	TPL_LINK	Tuple link
010H	02H	Conditions information	Tuple data
012H	D9H	Device information	Tuple data
014H	01H	Device information	Tuple data
016H	FFH	END MARKER	End of Tuple
018H	18H	CISTPL_JEDEC_C	Tuple code
01AH	02H	TPL_LINK	Tuple link
01CH	DFH	PCMCIA's manufacturer's JEDEC ID code	Tuple data
01EH	01H	PCMCIA's JEDEC device code	Tuple data
020H	20H	CISTPL_MANFID	Tuple code
022H	04H	TPL_LINK	Tuple link
024H	0AH	Low byte of manufacturer's ID code	Tuple data
026H	00H	High byte of manufacturer's ID code	Tuple data
028H	00H	Low byte of product code	Tuple data
02AH	00H	High byte of product code	Tuple data
02CH	15H	CISTPL_VERS_1	Tuple code
02EH	13H	TPL_LINK	Tuple link
030H	04H	TPLLV1_MAJOR	Tuple data
032H	01H	TPLLV1_MINOR	Tuple data
034H	50H	'P ' (Vender Specific Strings)	Tuple data
036H	48H	' H ' (Vender Specific Strings)	Tuple data
038H	49H	' I ' (Vender Specific Strings)	Tuple data
03AH	53H	'S ' (Vender Specific Strings)	Tuple data
03CH	4FH	' O ' (Vender Specific Strings)	Tuple data
03EH	4EH	'N ' (Vender Specific Strings)	Tuple data
040H	00H	Null Terminator	Tuple data
042H	43H	'C ' (Vender Specific Strings)	Tuple data

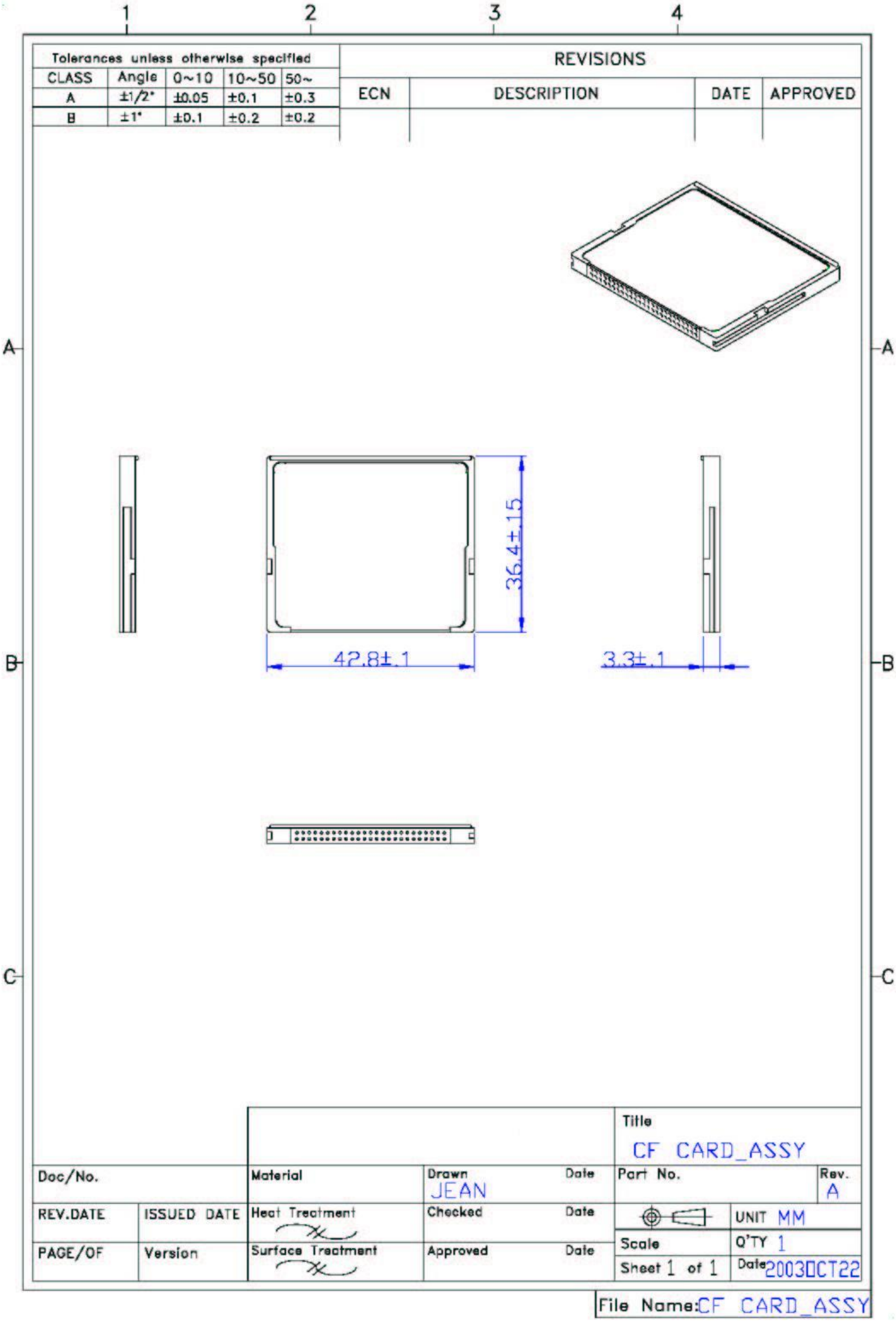
Address	Data	Description of Contents	CIS Function
044H	46H	‘ F ’ (Vender Specific Strings)	Tuple data
046H	20H	‘ ’ (Vender Specific Strings)	Tuple data
048H	43H	‘ C ’ (Vender Specific Strings)	Tuple data
04AH	61H	‘ a ’ (Vender Specific Strings)	Tuple data
04CH	72h	‘ r ’ (Vender Specific Strings)	Tuple data
04EH	64H	‘ d ’ (Vender Specific Strings)	Tuple data
050H	00H	Null Terminator	Tuple data
052H	00H	Reserved (Vender Specific Strings)	Tuple data
054H	FFH	END MARKER	End of Tuple
056H	21H	CISTPL_FUNCID	Tuple code
058H	02H	TPL_LINK	Tuple link
05AH	04H	IC Card function code	Tuple data
05CH	01H	System initialization bit mask	Tuple data
05EH	22H	CISTPL_FUNCE	Tuple code
060H	02H	TPL_LINK	Tuple link
062H	01H	Type of extended data	Tuple data
064H	01H	Function information	Tuple data
066H	22H	CISTPL_FUNCE	Tuple code
068H	03H	TPL_LINK	Tuple link
06AH	02H	Type of extended data	Tuple data
06CH	0CH	Function information	Tuple data
06EH	0FH	Function information	Tuple data
070H	1AH	CISTPL_CONFIG	Tuple code
072H	05H	TPL_LINK	Tuple link
074H	01H	Size field	Tuple data
076H	03H	Index number of last entry	Tuple data
078H	00H	Configuration register base address (Low)	Tuple data
07AH	02H	Configuration register base address (High)	Tuple data
07CH	0FH	Configuration register present mask	Tuple data
07EH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
080H	08H	TPL_LINK	Tuple link
082H	C0H	Configuration Index Byte	Tuple data
084H	C0H	Interface Descriptor	Tuple data
086H	A1H	Feature Select	Tuple data
088H	01H	Vcc Selection Byte	Tuple data
08AH	55H	Nom V Parameter	Tuple data
08CH	08H	Memory length (256 byte pages)	Tuple data

Address	Data	Description of Contents	CIS Function
08EH	00H	Memory length (256 byte pages)	Tuple data
090H	20H	Misc features	Tuple data
092H	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
094H	06H	TPL_LINK	Tuple link
096H	00H	Configuration Index Byte	Tuple data
098H	01H	Feature Select	Tuple data
09AH	21H	Vcc Selection Byte	Tuple data
09CH	B5H	Nom V Parameter	Tuple data
09EH	1EH	Nom V Parameter	Tuple data
0A0H	4DH	Peak I Parameter	Tuple data
0A2H	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0A4H	0AH	TPL_LINK	Tuple link
0A6H	C1H	Configuration Index Byte	Tuple data
0A8H	41H	Interface Descriptor	Tuple data
0AAH	99H	Feature Select	Tuple data
0ACH	01H	Vcc Selection Byte	Tuple data
0AEH	55H	Nom V Parameter	Tuple data
0B0H	64H	I/O Parameter	Tuple data
0B2H	F0H	IRQ parameter	Tuple data
0B4H	FFH	IRQ request mask	Tuple data
0B6H	FFH	IRQ request mask	Tuple data
0B8H	20H	Misc features	Tuple data
0BAH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0BCH	06H	TPL_LINK	Tuple link
0BEH	01H	Configuration Index Byte	Tuple data
0C0H	01H	Feature Select	Tuple data
0C2H	21H	Vcc Selection Byte	Tuple data
0C4H	B5H	Nom V Parameter	Tuple data
0C6H	1EH	Nom V Parameter	Tuple data
0C8H	4DH	Peak I parameter	Tuple data
0CAH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0CCH	0FH	TPL_LINK	Tuple link
0CEH	C2H	Configuration Index Byte	Tuple data
0D0H	41H	Interface Descriptor	Tuple data
0D2H	99H	Feature Select	Tuple data
0D4H	01H	Vcc Selection Byte	Tuple data
0D6H	55H	Nom V Parameter	Tuple data

Address	Data	Description of Contents	CIS Function
0D8H	EAH	I/O parameter	Tuple data
0DAH	61H	I/O range length and size	Tuple data
0DCH	F0H	Base address	Tuple data
0DEH	01H	Base address	Tuple data
0E0H	07H	Address length	Tuple data
0E2H	F6H	Base address	Tuple data
0E4H	03H	Base address	Tuple data
0E6H	01H	Address length	Tuple data
0E8H	EEH	IRQ parameter	Tuple data
0EAH	20H	Misc features	Tuple data
0ECH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0EEH	06H	TPL_LINK	Tuple link
0F0H	02H	Configuration Index Byte	Tuple data
0F2H	01H	Feature Select	Tuple data
0F4H	21H	Vcc Selection Byte	Tuple data
0F6H	B5H	Nom V Parameter	Tuple data
0F8H	1EH	Nom V Parameter	Tuple data
0FAH	4DH	Peak I Parameter	Tuple data
0FCH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0FEH	0FH	TPL_LINK	Tuple link
100H	C3H	Configuration Index Byte	Tuple data
102H	41H	Interface Descriptor	Tuple data
104H	99H	Feature Select	Tuple data
106H	01H	Vcc Selection Byte	Tuple data
108H	55H	Nom V Parameter	Tuple data
10AH	EAH	I/O parameter	Tuple data
10CH	61H	I/O range length and size	Tuple data
10EH	70H	Base address	Tuple data
110H	01H	Base address	Tuple data
112H	07H	Address length	Tuple data
114H	76H	Base address	Tuple code
116H	03H	Base address	Tuple link
118H	01H	Address length	Tuple data
11AH	EEH	IRQ parameter	Tuple data
11CH	20H	Misc features	Tuple data
11EH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
120H	06H	TPL_LINK	Tuple link

Address	Data	Description of Contents	CIS Function
122H	03H	Configuration Index Byte	Tuple data
124H	01H	Feature Select	Tuple data
126H	21H	Vcc Selection Byte	Tuple data
128H	B5H	Nom V Parameter	Tuple data
12AH	1EH	Nom V Parameter	Tuple data
12CH	4DH	Peak I Parameter	Tuple data
12EH	14H	CISTPL_NO_LINK	Tuple code
130H	00H	TPL_LINK	Tuple link
132H	FFH	CISTPL_END	End of Tuple
134H	FFH	CISTPL_END	End of Tuple
136H	FFH	CISTPL_END	End of Tuple
138H	FFH	CISTPL_END	End of Tuple
13AH	FFH	CISTPL_END	End of Tuple

7. PHYSICAL DIMENSION



8. REFERENCES

The following table is to list out the standards that have been adopted for designing the product.

Table 8-1 List of References

Title	Acronym/Source
RoHS	Restriction of Hazardous Substances Directive; for further information, please contact us at sales@phison.com or support@phison.com.
CompactFlash™ Card	http://www.compactflash.org/
PC Card Standard Release 8.0	http://www.compactflash.org/
ATA-8 spec	http://www.t13.org
FCC: CISPR22	Federal Communications Commission; for further information, please contact us at sales@phison.com or support@phison.com.
CE: EN55022	Consumer electronics certification; for further information, please contact us at sales@phison.com or support@phison.com.
BSMI: 13438	The Bureau of Standards, Metrology and Inspection; for further information, please contact us at sales@phison.com or support@phison.com.

9. TERMINOLOGY

The following table is to list out the acronyms that have been applied throughout the document.

Table 9-1 List of Terminology

Term	Definitions
LBA	Logical block addressing
MB	Mega-byte
MTBF	Mean time between failures
PATA	Parallel advanced technology attachment
SDR	Synchronous dynamic access memory
S.M.A.R.T.	Self-monitoring, analysis and reporting technology
SSD	Solid state disk